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(54) Adiabatic charging logic circuit

(57) An adiabatic charging logic circuit includes a logic circuit and a power supply section. The logic circuit is constituted by a plurality of logic elements. The power supply section supplies power to the logic circuit to cause the logic circuit to perform logic processing after an input signal is supplied to the gate of each of the logic elements, and stops supply of the power before a new input signal is supplied to the gate of each of the logic elements after completion of the logic processing.

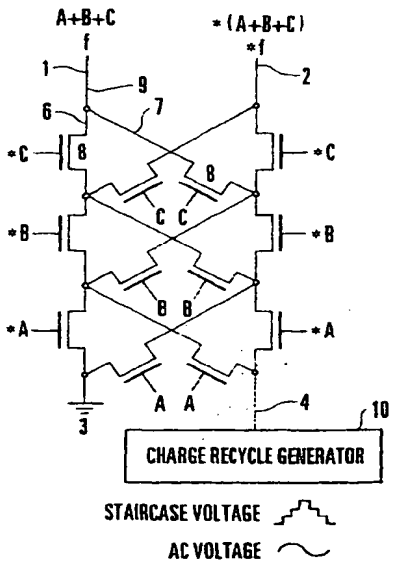


FIG. 1

EP 0 901 230 A1

Description

Background of the Invention

[0001] The present invention relates to a logic circuit such as a BDD logic circuit or D latch logic circuit which greatly reduces the power consumption and the circuit size by performing adiabatic charging logic using a supply voltage whose waveform moderately rises and falls.

[0002] An adiabatic charging logic method has received attention as a method of performing logic processing with low power consumption. One of the characteristics of this adiabatic charging logic method is that the supply voltage moderately and periodically changes (moderately rises and falls).

[0003] Assume that the supply voltage rises from Low (low voltage level) to High (high voltage level) sufficiently slowly as compared with the RC time constant of an inverter Serving as a logic circuit. In this case, it is known that the work done by the supply voltage is $1/2 \cdot CV^2$, which coincides with the energy stored in a load capacitance. It is also known that when the supply voltage changes from High to Low, the energy stored in the load capacitance is not discharged to ground (GND) but returns to the power supply circuit (charger recycling), thereby ideally performing logic processing of "Low → High → Low" with almost no consumption of energy (reference 1: "Energy-Recovery CMOS" William C. Athas, LOW POWER DESIGN METHODOLOGIES, edited by J. M. Rabaey et al., KLUWER ACADEMIC PUBLISHERS, pp. 66 - 72, 1996).

[0004] As a power supply circuit for implementing this logic, an AC circuit using an inductor and a capacitor are available. The inductor and the capacitor constitute a resonance circuit to generate an AC voltage. By using this circuit as a charge recycle generator, adiabatic charging and charge recycling can be performed.

[0005] A circuit that uses N - 1 capacitors to generate an N-step staircase voltage (a voltage that changes/rises in N steps and changes/falls in N steps) is also known (reference 1). With this circuit as well, adiabatic charging and charge recycling can be performed.

[0006] When, however, adiabatic charging or charge recycling is to be performed in a general CMOS circuit by using a charge recycle generator, even if the rise/fall timing of an output voltage from the charge recycle generator is properly adjusted for one logic gate, the rise/fall timing must be adjusted again for the logic gate on the next stage.

[0007] A transmission gate type retractile logic circuit, which differs from the above CMOS circuit but is known as a circuit capable of easily realizing adiabatic charging and charge recyding, will be described below as an example of how the timing is difficult to adjust.

[0008] Fig. 63A shows this retractile logic circuit. Reference numerals 501 to 504 denote logic gates; and 505 and 506, capacitors. This circuit receives input signals A and B, performs AND logic (= A • B) processing for the input signals, and obtains the OR logic (= A • B + C) of the AND logic processing result and an input signal C. As a logic gate of this retractile logic circuit, a two-wire logic element using transmission gates 507 has been proposed, as shown in Figs. 64B and 64C. This element receives complementary input signals A and *A and complementary input signals B and *B and outputs output signals A • B and *(A • B). Note that the symbol "*" indicates that the corresponding signal is an inverted signal.

[0009] In this retractile logic circuit, the waveforms of supply voltage V1 and V2 are controlled in accordance with the number of gates, as shown in the timing charts of Figs. 63B to 63F. More specifically, control must be performed to cause the supply voltage V1 to moderately (with a constant slope) rise later and fall earlier than the input signals A and B. The same applies to the relationship between the input signal C and the supply voltage V2.

[0010] Figs. 65A and 65B show a conventional BDD logic circuit. As shown in Fig. 65A, the BDD graph (Binary Decision Diagram) used for this logic circuit is a graph having beginning points 1 and 2 and ending points 3 and 4. Input variables (A, B, and C in Fig. 65A) correspond to nodes 5. When the value of a logic output is to be obtained from supplied input variable values, the input enters from the beginning point 1 or 2 of the graph, goes down along the respective nodes 5, and reaches one of the two ending points 3 and 4. At each node 5, the input goes along one of two branches 6 and 7 in accordance with the input variable value. If, for example, the input variable C is "0", the input goes along 0 branch 6. If C = "1", the input goes along 1 branch 7. That is, when an input is supplied, one path from a beginning point to an ending point is designated. If the ending point of the path is "0", the logic output becomes "0". If the ending point is "1", the logic output becomes "1".

[0011] In the BDD logic circuit, as shown in Fig. 65B, logic elements that satisfy the above conditions, e.g., N-channel MOSFETs 8 and wires 9, are made to correspond to the respective branches of the BDD on the basis of the BDD graph shown in Fig. 65A. In addition, logic outputs are made to correspond to the beginning points 1 and 2 of the BDD graph. Furthermore, ground (GND) is connected to the ending point 3 of "0" of the BDD graph, and a constant supply voltage VDD is connected to the ending point 4 of "1" of the BDD graph (reference 2: Kuroda and Sakurai, "Overview of Low-Power ULSI Circuit Techniques" IEICE TRANS. ELECTRON., Vol. E78-C, NO. 4 April 1995, pp. 334 - 344).

[0012] Fig. 66 shows the arrangement of a conventional D latch logic circuit. This logic circuit is made up of two transmission gates 601 and 602 constituting a data receiving circuit, and transmission gates 603 and 604 and inverters 605 and 606 which are cross-connected to constitute a storage circuit A clock signal CK and an inverted signal *CK thereof are input to the transmission gates 601 to 604, and constant supply voltages VDD

are applied to the inverters 605 and 606.

[0013] In this D latch logic circuit, when the clock signal CK is at High, the signals input to nodes 607 and 608 respectively reach nodes 609 and 610 through the transmission gates 601 and 602 and are inverted by the inverters 605 and 606. The resultant signals are then output to nodes 611 and 612. When the clock signal CK changes to Low, the nodes 610 and 611 are connected to each other, and the nodes 609 and 612 are connected to each other. As a result, the output signals from the inverters 605 and 606 are supplied to the input sides of the inverters 605 and 606 on the opposite sides. The output signals are held until the clock signal CK is set at High again (storage mode).

[0014] A wire 400 in Fig. 67, which is used in a conventional CMOS logic circuit such as a combinational logic circuit or a D latch logic circuit, has a large cross-sectional area to drive the gate on the next stage at high speed on the order of ps. As shown in Fig. 67, this wire cross-sectional area is 550 nm (0.55 μm: signal wire width W_0) x 550 nm (0.55 μm: signal wire thickness H_0) in the 0.25-μm process of Nippon Telegraph and Telephone Corporation (NTT). In this case, the CR time constant is about 0.5 ns.

[0015] In the above retractile logic circuit, as the number of gates increase to several hundreds and several thousands, several hundred and several thousand supply voltage waveforms must be controlled. If, therefore, adiabatic charging and charge recycling are performed by using a charge recycle generator, the power consumption increases contrarily.

[0016] In the D latch logic circuit, at a transmission gate portion, charging/discharging must be performed with respect to the gate of a MOSFET as an element of the transmission gate or a clock signal line. In this charging/discharging operation, the energy corresponding to $C_{TG}VDD^2$ (where VDD is the supply voltage and C_{TG} is the sum of the gate capacitance of the transmission gate and the capacitance of the clock signal line) is consumed. In the storage circuit as well, the energy corresponding to $C_{ME}VDD^2$ (where C_{ME} is the capacitance of the storage circuit) is consumed.

[0017] In the conventional CMOS logic circuit, since the wire cross-sectional area is set to be large, it is difficult to reduce the circuit size. In addition, the self-capacitance of each wire and the mutual capacitance between the wires cannot be reduced.

Summary of the Invention

[0018] The present invention has been made in consideration of the above situation, and its major object is to provide a logic circuit which can efficiently implement adiabatic charging logic, and can decrease the cross-sectional area of each wire, thereby realizing reductions in power consumption of the circuit and circuit size.

[0019] In order to achieve the above object, according to the present invention, there is provided an adiabatic charging logic circuit comprising a logic circuit constituted by a plurality of logic elements, and a power supply section for supplying power to the logic circuit to cause the logic circuit to perform logic processing after an input signal is supplied to a gate of each of the logic elements, and stopping supply of the power before a new input signal is supplied to the gate of each of the logic elements after completion of the logic processing.

Brief Description of the Drawings

[0020]

Fig. 1 is a circuit diagram showing a BDD logic circuit according to the first embodiment;

Fig. 2 is a circuit diagram showing a case wherein an AC power supply circuit is used as a charge recycle generator for the BDD logic circuit in Fig. 1;

Fig. 3 is a circuit diagram showing a case wherein a power supply circuit for generating a staircase voltage is used as a charge recycle generator for the BDD logic circuit in Fig. 1;

Figs. 4A to 4F are charts showing different voltage waveforms each used as the waveform of a voltage from the charge recycle generator and the like;

Fig. 5 is a circuit diagram showing a case wherein charge recycle generators are respectively used as power supply circuits for a plurality of BDD logic circuits;

Fig. 6 is a circuit diagram showing a case wherein a plurality of BDD logic circuits are formed into two groups, and a common charge recycle generator is used for each group;

Fig. 7 is a circuit diagram showing a BDD logic circuit according to the second embodiment;

Fig. 8 is a circuit diagram showing a case wherein a power supply circuit for generating a staircase voltage is used as a charge recycle generator for the BDD logic circuit in Fig. 7;

Figs. 9A to 9H are timing charts showing the operation of the power supply circuit in Fig. 8;

Figs. 10A to 10F are circuit diagrams showing arrangements for generating timing signals for the power supply circuit in Fig. 8;

Fig. 11 is a timing chart showing the simulation result obtained by using the power supply circuit in Fig. 8;

Fig. 12 is a timing chart showing the simulation result obtained by using the BDD logic circuit in Fig. 8;

Fig. 13 is a circuit diagram showing a BDD logic circuit according to the third embodiment;

Fig. 14 is a circuit diagram showing a BDD logic circuit according to the fourth embodiment;

Figs. 15A to 15D are circuit diagrams showing the circuit in Fig. 14 in more detail;

Fig. 16 is a timing chart showing the simulation result obtained by using the BDD logic circuit in

Figs. 15A to 15D;

Figs. 17A to 17G are circuit diagrams showing a BDD logic circuit according to the fifth embodiment;

Figs. 18A to 18D are circuit diagrams showing a BDD logic circuit according to the sixth embodiment;

Fig. 19 is a timing chart showing the simulation result obtained by using the BDD logic circuit in Figs. 18A to 18D;

Figs. 20A to 20G are circuit diagrams showing a BDD logic circuit according to the seventh embodiment;

Figs. 21A to 21H are timing charts for explaining other waveforms generated by an AC power supply;

Figs. 22A and 22B are views showing a BDD logic circuit according to the eighth embodiment;

Fig. 23 is a circuit diagram showing the detailed arrangement of the BDD logic circuit to which a non-charge-recycling generator, in the following called "charge no recycle generator", is connected;

Fig. 24 is a view for explaining an IC card according to the ninth embodiment;

Fig. 25 is a sectional view showing part of a BDD logic circuit according to the 10th embodiment;

Figs. 26A to 26E are views for explaining a combined BDD graph applied to a BDD logic circuit according to the 11th embodiment;

Figs. 27A and 27B are circuit diagrams showing a BDD logic circuit according to the 11th embodiment;

Fig. 28 is a circuit diagram showing a BDD logic circuit according to the 12th embodiment;

Figs. 29A to 29C are circuit diagrams showing a BDD graph for a case wherein the BDD logic circuit in Fig. 28 is applied for computation of sums by a 2-bit adder, and a BDD logic circuit;

Figs. 30A to 30C are circuit diagrams showing a BDD graph for a case wherein the BDD logic circuit in Fig. 28 is applied for computation of carries by a 2-bit adder, and a BDD logic circuit;

Fig. 31 is a circuit diagram showing a case wherein a power supply circuit using an inductor is used as a charge recycle generator for the BDD logic circuit in Fig. 28;

Fig. 32 is a circuit diagram showing a case wherein a power supply circuit for generating a staircase voltage is used as a charge recycle generator for the BDD logic circuit in Fig. 28;

Fig. 33 is a circuit diagram showing a case wherein charge recycle generators are respectively used as power supply circuits for a plurality of BDD logic circuits;

Fig. 34 is a circuit diagram showing a case wherein a plurality of BDD logic circuits are formed into two groups, and a common charge recycle generator is used for each group;

Fig. 35 is a circuit diagram showing a BDD logic circuit according to the 13th embodiment;

Fig. 36 is a circuit diagram showing a BDD logic circuit according to the 14th embodiment;

Fig. 37 is a circuit diagram showing a BDD logic circuit according to the 15th embodiment;

Figs. 38A to 38D are circuit diagrams showing a detailed arrangement of the circuit in Fig. 37;

Figs. 39A to 39G are circuit diagrams showing a BDD logic circuit according to the 16th embodiment;

Figs. 40A to 40D are circuit diagrams showing a BDD logic circuit according to the 17th embodiment;

Figs. 41A to 41G are circuit diagrams showing a BDD logic circuit according to the 18th embodiment;

Figs. 42A and 42B are views for explaining a BDD logic circuit according to the 19th embodiment;

Fig. 43 is a circuit diagram showing a charge no recycle generator for the BDD logic circuit in Figs. 42A and 42B;

Figs. 44A to 44C are views for explaining a D latch logic circuit according to the 20th embodiment and the waveforms of supply voltages;

Figs. 45A and 45B are graphs for comparing/explaining charged/discharged energy at clock portions and storage circuit portions in the present invention and the prior art;

Fig. 46 is a circuit diagram showing a D latch logic circuit according to the 21st embodiment;

Figs. 47A to 47C are circuit diagrams showing circuits for generating signals A, B, and C in the circuit in Fig. 46;

Figs. 48A to 48H are timing charts showing voltage waveforms in the circuit in Fig. 46;

Figs. 49A to 49D are views for explaining a D latch logic circuit according to the 22nd embodiment and supply voltage waveforms;

Fig. 50 is a circuit diagram showing a D latch logic circuit according to the 23rd embodiment;

Figs. 51A to 51D are timing charts showing voltage waveforms in the circuit in Fig. 50;

Figs. 52A and 52B are circuit diagrams each showing a D latch logic circuit according to the 24th embodiment;

Figs. 53A to 53C are circuit diagrams showing a PMOS latch logic circuit according to the 25th embodiment;

Figs. 54A to 54C are circuit diagrams showing a PMOS latch logic circuit according to the 26th embodiment;

Fig. 55 is a block diagram showing a logic circuit according to the 27th embodiment;

Figs. 56A an 56B are circuit diagrams each showing a logic circuit according to the 27th embodiment;

Figs. 57A and 57B are circuit diagrams NMOS latch logic circuits according to the 28th and 29th embodiments;

Figs. 58A and 58B are circuit diagrams PMOS latch logic circuits according to the 30th and 31st embodiments;

Figs. 59A and 59B are circuit diagrams each showing a circuit according to the 32nd embodiment;

Figs. 60A to 60C are views for explaining the 33rd embodiment;

Figs. 61A to 61C are views for explaining the 34th embodiment;

Fig. 62 is a block diagram showing how power supply control is performed on a BDD logic circuit and D latch logic circuit;

Figs. 63A to 63F are views for explaining a conventional retractile logic circuit and waveforms in operation;

Figs. 64A to 64C are views for explaining how a retractile logic circuit is implemented;

Figs. 65A and 65B are circuit diagrams showing a conventional BDD logic circuit;

Fig. 66 is a circuit diagram showing a conventional D latch logic circuit; and

Fig. 67 is a view showing the cross-sectional area of a wire in a conventional CMOS logic circuit.

Description of the Preferred Embodiments

[0021] The present invention will be described below with reference to the accompanying drawings.

[First Embodiment]

[0022] In the first embodiment, after the logic based on several hundred or several thousand gates is implemented by performing adiabatic charging once using a power recycle generator in place of the constant supply voltage for the BDD logic circuit in Fig. 65B described above, which is a circuit based on a BDD graph, the charge stored in a BDD logic circuit is returned to a power supply circuit.

[0023] The above BDD graph will be described again with reference to Fig. 65A. The BDD graph is a graph having the beginning points 1 and 2 and the ending points 3 and 4. Input variables (A, B, and C in Fig. 65A) correspond to the respective nodes 5. When a logic output value is to be obtained from input variable values, each input variable comes into the beginning point 1 or 2, goes down through the respective nodes 5, and reaches the ending point 3 or 4. At each node 5, each input variable follows one of the two branches 6 and 7 in accordance with the input variable value. If, for example, the input variable is C = "0", the variable follows 0 branch 6. If C = "1", the variable follows 1 branch 7. That is, once an input is supplied, one path from the beginning point to the ending point is designated. If "0" is set at the ending point of the path, the logic output is "0". If "1" is set at the ending point, the logic output is "1".

[0024] In the BDD logic circuit according to the first embodiment of the present invention in Fig. 1, a logic element that satisfies the above condition, e.g., an n-channel MOSFET 8, and a wire 9 are caused to correspond to each branch of the BDD graph. Logic outputs are made to correspond to beginning points 1 and 2 of the BDD graph. In addition, ground (GND) is connected to a beginning point 3 of "0" of the BDD graph, and a charge recycle generator 10 is connected to a beginning point 4 of "1" of the BDD graph. As this charge recycle generator 10, as will be described later, for example, an AC power supply circuit using an inductor and a capacitor, or a power supply circuit using N - 1 capacitors and serving to generate an N-step staircase voltage is used.

[0025] The timing of power supply from this charge recycle generator 10 to a BDD logic circuit and a D latch logic circuit (to be described later) is controlled by a timing control section 450, as shown in Fig. 62. Note that a BDD logic circuit 30A in Fig. 62 corresponds to the BDD logic circuit shown in Fig. 1 or 2 or the like, and a BDD logic circuit 30B in Fig. 62 corresponds to the BDD logic circuit shown in Fig. 28 and the subsequent drawings to be described later. Recycling operation using the charge recycle generator 10 (#2) at the gate portion of the BDD logic circuit will be described later in the fourth , fifth, sixth, and seventh embodiments.

[0026] Fig. 2 shows an AC power supply circuit 10A using an inductor 11 and a capacitor 12. Fig. 3 shows a power supply circuit 10B for generating a 4-step staircase voltage by using three capacitors 13 to 15.

[0027] Referring to Fig. 3, reference numerals 16 to 23 denote n-channel MOSFETs. These power supply circuits 10A and 10B can generate output voltages having AC waveforms (repetitive waveforms) that moderately rise and fall. Note that as other types of AC voltages generated by the charge recycle generator, the triangular wave shown in Fig. 4A and the trapezoidal wave shown in Fig. 4B can be used. In addition, the voltage waveforms generated from the sine waves respectively shown in Figs. 4C, 4D, and 4E can be used. Note that generation of a triangular wave can be approximately performed by causing, for example, a voltage having a staircase waveform to pass through an integrating circuit.

[0028] The operation of a BDD logic circuit 30A shown in Fig. 1 will be described next. First of all, at time t = 0, input voltages *A, *B, *C, A, B, and C are respectively input to the gates of the n-channel MOSFETs 8. The output voltage from the charge recycle generator 10 is then moderately raised. With this operation, the BDD logic circuit can be adiabatically charged. With this charging, logic operation is performed to obtain an output signal. After this adiabatic charging operation, the output voltage from the charge recycle generator 10 is moderately lowered. At this time, the charge stored in the BDD logic circuit is returned to the charge recycle generator 10 again. At time t = T after the output potential of the BDD logic circuit is set at Low, the next input signals are input to the gates. By repeating this opera-

tion at periods T, adiabatic charging and charge recycling can be executed.

[0029] As described above, even if the number of gates increases to several hundreds or several thousands, since the common charge recycle generator 10 is used, the power consumption does not increase, and low power consumption can be realized even in a logic circuit having a complicated logic structure, unlike a conventional retractile logic circuit.

[0030] Fig. 4F is a graph showing a comparison between the power consumption in the power supply section of the BDD logic circuit of the present invention and that of the conventional retractile logic circuit. As is obvious from this graph, in the conventional retractile logic circuit, as the number of gates of the logic circuit increases, the power consumption increases. In contrast to this, in the BDD logic circuit of the present invention, the power consumption is constantly kept low.

[0031] Fig. 5 shows an arrangement including a plurality of BDD logic circuits. Assume that this arrangement includes n BDD logic circuits 30_1 to 30_n ($n \geq 4$), and the ith and jth BDD logic circuits are adjacent to each other ($j = i + 1$). In this case, the respective BDD logic circuits are independently operated by optimal charge recycle generators 10_1 to 10_n. For example, as the power supply for the kth BDD logic circuit, a charge recycle generator with a frequency f_k and a phase ϕ_k is used. Each BDD logic circuit requiring fast logic operation uses a charge recycle generator having an increased frequency f_k, whereas each BDD logic circuit that does not require fast logic operation uses a charge recycle generator having a decreased frequency f_k. This allows the respective BDD logic circuits to efficiently perform concurrent processing.

[0032] In addition, BDD logic circuits that can use supply voltages having the same frequency and the same phase share a charge recycle generator through power lines to decrease the number of power supply circuits, thereby realizing low power consumption.

[0033] Fig. 6 shows an arrangement using common charge recycle generators. In this circuit arrangement, the 1st to ith supply voltages are applied from a common charge recycle generator 10_1, and the jth to nth supply voltages are applied from a common charge recycle generator 10_n.

[Second Embodiment]

[0034] Fig. 7 shows a BDD logic circuit according to the second embodiment of the present invention.

[0035] In the arrangement shown in Fig. 7, of the n-channel MOSFETs 8 serving as logic elements in the BDD logic circuit shown in Fig. 1, the elements whose gates receive the inverted signals *A, *B, and *C as input signals are replaced with logic elements that are complementary to those in Fig. 1. More specifically, the logic elements in Fig. 1 are replaced with p-channel MOSFETs 24, and non-inverted signals A, B, and C are used as input signals to the gates of the p-channel MOSFETs 24. With this arrangement, since only the non-inverted signals A, B, and C can be used as input signals, one inverter for inverting a non-inverted signal can be omitted from each logic element. This circuit can therefore achieve lower power consumption than the BDD logic circuit shown in Fig. 1. Note that the same applies to each of the BDD logic circuits in Figs. 2, 3, 5, and 6.

[0036] An example of the operation of the BDD logic circuit in Fig. 7, which uses n-channel MOSFETs 8 and the p-channel MOSFETs 24 together, will be described in detail below by using simulation results. In this case, as a charge recycle generator, a power supply 10B (identical to the one shown in Fig. 3) designed to generate a 4-step staircase voltage by using three capacitors 13 to 15.

[0037] This charge recycle generator 10B is constituted by four constant supply voltages VDD, 3/4VDD, 2/4VDD, and 1/4VDD, three capacitors 13 to 15, and eight n-channel MOSFETs 16 to 23. The three capacitors 13 to 15 are respectively charged by the voltages 3/4VDD, 2/4VDD, and 1/4VDD. Input signals Pre are applied to the gates of the three n-channel MOSFETs 16 to 18. Input signals T1 to T4 are respectively applied to the gates of the four n-channel MOSFETs 19 to 22. An input signal CL is applied to the gate of the one n-channel MOSFET 23. Although the capacitors 13, 14, and 15 are naturally charged to 3/4VDD, 2/4VDD, and 1/4VDD without the voltages 3/4VDD, 2/4VDD, and 1/4VDD, respectively, to become stable, a circuit arrangement like the one shown in Fig. 10B is employed in consideration of the need for fast charging operation.

[0038] Figs. 9A to 9H show the operation of the charge recycle generator 10B in detail. First of all, the input signal Pre in Fig. 9A is kept High for a predetermined period of time to turn on the n-channel MOSFETs 16 to 18, thereby charging the capacitors 13 to 15 to the voltages 3/4VDD, 2/4VDD, and 1/4VDD, respectively. Then, each of the input signals T1 to T4 in Figs. 9E to 9H is kept High for a predetermined period of time in the order of T1 → T2 → T3 → T4 → T3 → T2 → T1 to turn on the n-channel MOSFETs 19 to 22 so as to time-divisionally output the voltages 3/4VDD, 2/4VDD, and 1/4VDD charged in the capacitors 13 to 15 as an output voltage Vout. Finally, when the input signal T1 is set at Low, the input signal CL is set at High, and the n-channel MOSFET 23 is kept on for a predetermined period of time, thereby setting the output voltage Vout to the ground potential. With this timing control, the waveform of the output voltage Vout from the charge recycle generator 10B has four steps at leading and trailing edges, as shown in Fig. 9C.

[0039] The above input signals (pulses) CL, T1, T2, T3, and T4 can be generated by, for example, a circuit using three T-type flip-flop circuits 41 to 43, 11 NAND circuits 44 to 54, and three inverters 55 to 57, as shown in Figs. 10A to 10F. Referring to Figs. 10A to 10F, refer-

ence numeral 200 denotes an input terminal for a predetermined clock CK; 211, an output terminal for the signal T1; 212, an output terminal for the signal T2; 213, an output terminal for the signal T3; 214, an output terminal for the signal T4; and 215, an output terminal for the signal CL. Other reference numerals denote nodes, and the nodes denoted by the same reference numeral are commonly connected.

[0040] In performing a simulation, the capacitance of each of the capacitors 13 to 15 of the charge recycle generator 10B was set to 5,000 pF, and the transistor width W of each of the eight n-channel MOSFETs 16 to 23 was set to 36 μm. In addition, in each 3-input XOR BDD logic circuit in Fig. 8, the transistor width W was set to 6 μm, and the load capacitance of the output on the XOR side was set to 0.5 pF. In this case, the simulation was performed for a parallel circuit of 1,000 3-input XOR BDD logic circuits. The frequency of the input clock CK was set to 4 MHz. Figs. 11 and 12 show the simulation results.

[0041] Fig. 11 shows the waveforms of the signals Pre, CK, CL, T1 to T4, and Vout in the charge recycle generator 10B. Obviously, desired waveforms like those shown in Figs. 9A to 9H are obtained. Since the sum total of the output loads is 1,000 times 0.5 pF (= 500 pF), the resultant waveform is slightly smoother than the staircase waveform.

[0042] Fig. 12 shows the waveforms of the input signals A, B, and C, the supply voltage Vout, and output signals XOR and XNOR. As described above, input voltages are switched when the supply voltage Vout is at Low level. If each of the input signals A, B, and C is "1", XOR and XNOR become "1" and "0", respectively. If A = B = "1" and C = "0", XOR and XNOR become "0" and "1", respectively. That is, logic processing is properly performed. The pulse width (bit width) of the signal C is 2 μs, and the frequency of the output voltage is set 500 kHz.

[0043] In addition, the power consumption becomes 4.76×10^{-4} W at a frequency of 500 kHz. On the other hand, the power consumption per unit logic processing in one XOR circuit of a general CMOS is 1.06×10^{-6} W, and hence the power consumption per unit logic processing in 1,000 XOR circuits is 1.06×10^{-3} W. As is obvious, with the use of the circuit of the present invention, the power consumption can be reduced to 1/2 of that of the general CMOS logic circuit. It can be confirmed from the above argument that the BDD logic circuit using the charge recycle generator according to the present invention can realize lower power consumption.

[Third Embodiment]

[0044] Fig. 13 shows a BDD logic circuit using a charge recycle generator according to the third embodiment of the present invention. In this case, the n-channel MOSFETs 8 serving as logic elements in the BDD logic circuit shown in Fig. 1 are replaced with transmission gates 81 each formed by connecting an n-channel MOSFET and a p-channel MOSFET in parallel with each other. An input signal to each p-channel MOSFET is the inverted signal of an input signal to a corresponding n-channel MOSFET. With this arrangement, since a High-level signal obtained as an output signal rises from VDD-Vth (Vth is the threshold voltage of an n-channel MOSFET) to a supply voltage VDD, the voltage amplitude of the logic signal can be set to be large as compared with the circuit shown in Fig. 1. In an n-channel MOSFET, the propagation characteristic of a Low-level signal is good, but a High-level signal undergoes a voltage drop corresponding to the threshold voltage during propagation. This arrangement can Prevent this. In a p-channel MOSFET, the propagation characteristic of a High-level signal is good, but that of a Low-level signal is poor. The transmission gates can solve these problems.

[Fourth Embodiment]

[0045] Fig. 14 shows a BDD logic circuit using a charge recycle generator according to the fourth embodiment. As this charge recycle generator, an AC power supply is used. To recycle the charge stored in the input gates, AC voltages Aac, Bac, and Cac, each having the same frequency and phase as those of an AC supply voltage V1ac, are applied to the input gates of the logic elements.

[0046] Figs. 15A to 15D show a detailed circuit arrangement obtained by combining the circuit in Fig. 14 with inverters 25 to 27. In this case, the AC supply voltage V1ac is used as a supply voltage applied to the BDD logic circuit. The supply voltage applied to the inverter 25 for receiving an inverted signal *A and outputting a noninverted signal A is also the AC supply voltage V1ac, so is the supply voltage applied to each of the remaining inverters 26 and 27. In this case, as V1ac, a sine-wave voltage having an offset of 1 V (center voltage of 1 V) and an amplitude of 1 V are used. In addition, as each of inverted signals *A, *B, and *C, a signal whose Low and High levels are respectively set to 0 V and 2 V is used.

[0047] Fig. 16 shows the simulation result obtained when the operating speed was set to 500 kHz. Fig. 16 shows the waveforms of the AC voltage V1ac, the input signals *A, A, *B, B, *C, and C, and output signals XOR and XNOR.

[0048] 2 V (peak) and 0 V of the AC voltage respectively correspond to High level ("1") and Low level ("0") of the input signal A. Obviously, the signals A, B, and C respectively represent "111100001", "110011001", and "101010101" in the time interval between 7 μs and 25 μs. In addition, when A = B = C = "1", XOR is "1". When A = B = "1" and C = "0", XOR is "0". The power consumption of the BDD logic circuit is 2.71×10^{-7} W. The power consumption of this AC BDD logic circuit is about 1/4 of that of a CMOS.

[0049] Although the sine-wave voltage is used as an AC voltage, the AC voltage is not limited to this. For example, as the voltage V1ac, a voltage having a triangular wave, a trapezoidal wave, or one of the voltage waveforms generated from a sine wave, which are shown in Figs. 4A to 4E, can be used. As is obvious, a staircase voltage waveform (Vout in Fig. 9C) obtained by the power supply circuit 10B shown in Fig. 8 can also be used.

[Fifth Embodiment]

[0050] Figs. 17A to 17G show a BDD logic circuit using a charge recycle generator according to the fifth embodiment. In this case, when an AC power supply V1ac is used as a charge recycle generator for the BDD logic circuit shown in Fig. 13, a circuit obtained by connecting transmission gates 81 in series with each other is used instead of each of the inverters 25 to 27 in Figs. 15A to 15C. As shown in Figs. 17A and 17B, the circuit receives logic signals Ain and *Ain and generates AC voltage signals A and *A. As shown in Figs. 17C and 17D, the circuit receives logic signal Bin and *Bin and generates AC voltage signals B and *B. In addition, as shown in Figs. 17E and 17F, the circuit receives logic signals Cin and *Cin and generates AC voltage signals C and *C. These AC voltages A, *A, B, *B, C, and *C are input to the BDD logic circuit to perform logic processing.

[Sixth Embodiment]

[0051] Figs. 18A to 18D show a BDD logic circuit using a charge recycle generator according to the sixth embodiment, in which an AC voltage V1ac is used as an input voltage, and an AC voltage V2ac' is used for a charge recycle generator. This AC voltage V2ac' has a frequency twice that of the AC voltage V1ac. In addition, an n-channel MOSFET 28 having a switching function is connected between the BDD logic circuit and the AC voltage V2ac'. By supplying a clock signal ϕ (having the same frequency as that of the AC signal V1ac) to the gate of this n-channel MOSFET 28, as shown in Fig. 18D, the peaks of the AC voltage V2ac' are alternately extracted, thereby obtaining an AC voltage V2ac as a supply voltage.

[0052] Fig. 19 shows a simulation result.

[0053] Fig. 19 shows the waveforms of the AC voltage V2ac', the clock signal ϕ, the AC voltage V2ac having passed through the n-channel MOSFET 28, the AC voltage V1ac, an input signal C, and output signals XOR and XNOR. Although input signals A and B are not shown, they have the same waveforms as those in Fig. 16. Obviously, the signals XOR and XNOR are properly output as in the simulation result shown in Fig. 16.

[0054] In this circuit, the power consumption is 3.6 x 10^{-8} W, which is about 1/30 of that of a CMOS. The reason for such low power consumption may be that since the waveform of the AC voltage V2ac from the power supply is fitted in the waveform of the input AC voltage V1ac, almost no leakage occurs from the power supply to ground.

[Seventh Embodiment]

[0055] Figs. 20A to 20G show a BDD logic circuit using a charge recycle generator according to the seventh embodiment, in which the above AC voltage V1ac is used as an input voltage, and an AC voltage V2ac' is used as a charge recycle generator for the BDD logic circuit shown in Fig. 17G. This AC voltage V2ac' has a frequency twice that of the AC voltage V1ac. A transmission gate is connected between the BDD logic circuit and the AC voltage V2ac'. By supplying a clock signal ϕ (having the same frequency as that of the AC signal V1ac) and a signal $\overline{\phi}$ to the transmission gate, as shown in Fig. 20G, the peaks of the AC voltage V2ac' are alternately extracted, thereby obtaining an AC voltage V2ac as a supply voltage.

[0056] In the seventh embodiment and the fifth and sixth embodiments, as described above, the AC voltage need not be a sine-wave voltage. For example, a voltage having a trapezoidal waveform or a staircase waveform obtained by a power supply circuit 10B may be used. In addition, the relationship in timing between the AC voltages V1ac and V2ac can be arbitrarily set as long as the voltage V1ac rises earlier and falls later than the voltage V2ac. Figs. 21A to 21H show several examples of this relationship.

[Eighth Embodiment]

[0057] Fig. 22A shows a BDD logic circuit according to the eighth embodiment. In this case, the charge recycle generator 10 of the BDD logic circuit shown in Fig. 1 is replaced with a non-charge-recycling or "charge no recycle" generator 10'. The charge no recycle generator 10' is an AC power supply (for generating a voltage that generally rises and falls and periodically changes) that does not recycle power. Fig. 22B shows the relationship between an AC power supply, the charge recycle generator 10, and the charge no recycle generator 10'.

[0058] Fig. 23 shows a circuit including the charge no recycle generator 10'. In this case, the rectangular wave output from an inverter 35 is integrated by a resistor 36 and a capacitor 37 to generate a repetitive voltage that moderately rises and falls. Such an AC power supply that does not recycle power cannot recycle the charge. However, since adiabatic charging can be performed, unlike a power supply using a rectangular wave, the power consumption can be reduced to 1/2.

[Ninth Embodiment]

[0059] Fig. 24 shows an IC card 60 according to the ninth embodiment. In this case, when there is an AC

voltage induced from a radio electromagnetic wave from a reader/writer 61 or the like used for communication (or power transmission) through an inductor (antenna) 62, this AC voltage itself is used as a charge recycle generator voltage for the IC card 60. Reference numeral 63 denotes a BDD logic circuit; 64, a rectifier power supply circuit for generating a DC supply voltage for a CMOS logic circuit 65; and 66, a capacitor. Reference symbol M denotes a transconductance.

[10th Embodiment]

[0060] Fig. 25 shows part of a BDD logic circuit according to the 10th embodiment, in which complementary TFTs (Thin Film Transistors) are used as logic elements in place of complementary MOSFETs. Fig. 25 shows a circuit arrangement using such TFTs. This circuit can perform adiabatic charging and charge recycling. Each TFT operates slower than each MOSFET, and hence is regarded as a device suitable for adiabatic charging.

[0061] A three-dimensional, high-integration circuit can be formed by using these TFTs. This circuit arrangement allows elements to be connected in parallel with each other in the direction of thickness, and hence can attain a high logic processing speed. Referring to Fig. 25, reference numeral 71 denotes a substrate; 72, an insulating film; 73, a metal or polysilicon wire or gate; 74, a gate insulating film; 75, an n-type region serving as a source or drain; 76, a p-type region serving as a channel; 77, a p-type region serving as a source or drain; 78, an n- type region serving as channel; and 79, a global through hole.

[0062] In this case, the complementary TFTs are used to implement the BDD logic circuits (Fig. 7, 8, 13, 14, 15D, 17G, 18D, 20G) used in the second to seventh embodiments. As is obvious, however, this arrangement can also be applied to the BDD logic circuit of the first embodiment, which is not complementary, in Figs. 1 to 3, 5, and 6.

[11th Embodiment]

[0063] Fig. 26E explains a BDD graph used for a BDD logic circuit according to the 11th embodiment of the present invention. The BDD graph shown in Fig. 26E is obtained by combining the BDD graphs shown in Figs. 26A to 26D.

[0064] Figs. 27A and 27B show BDD logic circuits using the combined BDD graph in Fig. 26E. By combining the respective BDD graphs in this manner, the number of transistors used for a BDD logic circuit can be decreased.

[12th Embodiment]

[0065] Fig. 28 shows the arrangement of a BDD logic circuit 30B according to the 12th embodiment of the present invention. This BDD logic circuit receives input signals A, *A, B, *B, C, and *C to extract carry outputs $f = (AB + BC + CA)$ and $*f = *(AB + BC + CA)$. In the BDD logic circuits 30B of the 12th embodiment and the subsequent embodiments, a charge recycle generator 10 is connected to a beginning point 1 to apply a supply voltage to it so as to respectively extract the output signals f and *f from "1" of an ending point 4 and "0" of an ending point 3. Note that the waveform of the voltage output from this charge recycle generator 10 includes, for example, a staircase waveform and an AC-like waveform (whose level smoothly changes without changing in polarity) like those shown in Figs. 4A to 4E and 9C.

[0066] Figs. 29A and 29B explain a case wherein two input signal bits A0 and A1, two input signal bits B0 and B1, and one carry bit C0 are input to a 2-bit adder 140 in Fig. 29C to output sum output signals S1 and *S1. In this case, Fig. 29A shows the BDD graph for this arrangement. Fig. 29B shows the logic circuit of the arrangement. Fig. 29C shows the relationship between the inputs and outputs of the adder 140.

[0067] Figs. 30A and 30B explain a case wherein two input signal bits A0 and A1, two input signal bits B0 and B1, and one carry bit C0 are input to a 2-bit adder 140 in Fig. 30C to output carry output signals C2 and *C2. In this case, Fig. 30A shows the BDD graph for this arrangement. Fig. 30B shows the logic circuit of the arrangement. Fig. 30C shows the relationship between the inputs and outputs of the adder 140.

[0068] In this case, as the charge recycle generator 10, an AC-like power supply circuit using an inductor, and a capacitor or a power supply circuit that uses N - 1 capacitors to generate an N-step staircase voltage can be used.

[0069] Fig. 31 shows an AC-like power supply circuit 10A using an inductor 11 and a capacitor 12.

[0070] Fig. 32 shows a power supply circuit 10B that uses three capacitors 13 to 15 to generate a 4-step staircase voltage. Referring to Fig. 32, reference numerals 16 to 23 denote n-channel MOSFETs. These power supply circuits 10A and 10B can make their output voltages moderately rise and fall.

[0071] The operation of the BDD logic circuit shown in Fig. 32 will be described next.

[0072] At time t = 0, the input signals *A, *B, *C, A, B, and C are input to the gates of the respective n-channel MOSFETs of the BDD logic circuit. The output voltage from the charge recycle generator 10B is then made to moderately rise. With this operation, the BDD logic circuit can be adiabatically charged. With this charging operation, logic operation is performed to obtain output signals. After the charging operation, the output voltage from the charge recycle generator 10B is made to moderately fall. At this time, the charge stored in the BDD logic circuit is returned to the charge recycle generator 10B. At time t = T after the potential of the BDD logic circuit is set at Low, the next input signals are input to the gates. Subsequently, this operation is repeated at

periods T to allow execution of adiabatic charging and charge recycling.

[0073] As described above, even if the number of gates increases to several hundreds or several thousands, since a common charge recycle generator is used, low power consumption can be realized even in a logic circuit having a complicated logic structure.

[0074] Since the detailed operation of the charge recycle generator 10B shown in Fig. 32 is the same as that described with reference to the timing charts of Figs. 9A to 9H, a description thereof will be omitted.

[0075] In addition, since circuits for generating the respective input signals to be supplied to the charge recycle generator 10B are identical to those generated by the circuits shown in Figs. 10A to 10F, a description thereof will be omitted.

[0076] Furthermore, this charge recycle generator 10B generates a voltage waveform identical to Vout in Fig. 9C described above, and applies it to the BDD logic circuit.

[0077] Fig. 33 shows an arrangement including a plurality of BDD logic circuits. Assume that this arrangement includes n BDD logic circuits 30_1 to 30_n ($n \geq 4$), and the ith and jth BDD logic circuits are adjacent to each other ($j = i + 1$). In this case, the respective BDD logic circuits are independently operated by optimal charge recycle generators 10_1 to 10_n. For example, as the power supply for the kth BDD logic circuit, a charge recycle generator with a frequency f_k and a phase ϕ_k is used. Each BDD logic circuit requiring fast logic operation uses a charge recycle generator having an increased frequency f_k, whereas each BDD logic circuit that does not require fast logic operation uses a charge recycle generator having a decreased frequency f_k. This allows the respective BDD logic circuits to efficiently perform concurrent processing.

[0078] In addition, BDD logic circuits that can use supply voltages having the same frequency and the same phase share a charge recycle generator through power lines to decrease the number of power supply circuits, thereby realizing low power consumption.

[0079] Fig. 34 shows an arrangement using common charge recycle generators. In this circuit arrangement, the 1st to ith supply voltages are applied from a common charge recycle generator 10_1, and the jth to nth supply voltages are applied from a common charge recycle generator 10_n.

[13th Embodiment]

[0080] Fig. 35 shows a BDD logic circuit according to the 13th embodiment. According to this embodiment, in the BDD logic circuit shown in Fig. 28, of the n-channel MOSFETs 8 as logic elements, elements having gates to which the inverted signals *A, *B, and *C in Fig. 28 are input as input signals are replaced with logic elements complementary to these elements. More specifically, these elements are replaced with p-channel MOSFETs 24, and noninverted signals A, B, and C are input as input signals to their gates. With this arrangement, since only the non-inverted signals A, B, and C can be used as input signals, one inverter for generating an inverted signal from a non-inverted signal can be omitted from each circuit. Therefore, a circuit smaller in size and lower in power consumption than the circuit shown in Fig. 28 can be realized. The same applies to the BDD logic circuits shown in Figs. 29B, 30B, 31, 32, 33, and 34.

[14th Embodiment]

[0081] Fig. 36 shows a BDD logic circuit using a charge recycle generator according to the 14th embodiment of the present invention. In this case, the n-channel MOSFETs 8 serving as logic elements in the BDD logic circuit shown in Fig. 28 are replaced with transmission gates 81 each formed by connecting an n-channel MOSFET and p-channel MOSFET in parallel with each other. An input signal to each p-channel MOSFET is the inverted signal of an input signal to a corresponding n-channel MOSFET. With this arrangement, since a High-level signal obtained as an output signal rises from VDD-Vth (Vth is the threshold voltage of an n-channel MOSFET) to a supply voltage VDD, the voltage amplitude of the logic signal can be set to be large as compared with the circuit shown in Fig. 28. In an n-channel MOSFET, the propagation characteristic of a Low-level signal is good, but a High-level signal undergoes a voltage drop corresponding to the threshold voltage during propagation. This arrangement can prevent this. In a p-channel MOSFET, the propagation characteristic of a High-level signal is good, but that of a Low-level signal is poor. The transmission gates can solve these problems.

[15th Embodiment]

[0082] Fig. 37 shows a BDD logic circuit using a charge recycle generator according to the 15th embodiment. As this charge recycle generator, an AC-like power supply is used. To recycle the charge stored in the input gates, AC-like voltages Aac, Bac, and Cac, each having the same frequency and phase as those of an AC-like supply voltage V1ac, are applied to the input gates of the logic elements.

[0083] Figs. 38A to 38D show a detailed circuit arrangement obtained by combining the circuit in Fig. 37 with inverters 25 to 27. In this case, the AC-like supply voltage V1ac is used as a supply voltage applied to the BDD logic circuit. The supply voltage applied to the inverter 25 for receiving an inverted signal *A and outputting a non-inverted signal A is also the AC-like supply voltage V1ac, so is the supply voltage applied to each of the remaining inverters 26 and 27. In this case, as V1ac, a sine-wave voltage having an offset of 1 V (center voltage of 1 V) and an amplitude of 1 V is used. In addition,

as each of inverted signals *A, *B, and *C, a signal whose Low and High levels are respectively set to 0 V and 2 V is used.

[0084] Although the sine-wave voltage is used as an AC-like voltage, the AC-like voltage is not limited to this. For example, as the voltage V1ac, a voltage having a triangular wave, a trapezoidal wave, or one of the voltage waveforms generated from a sine wave, which are shown in Figs. 4A to 4E, can be used. As is obvious, a staircase voltage waveform (Vout in Fig. 9C) obtained by the power supply circuit 10B shown in Fig. 8 can also be used.

[16th Embodiment]

[0085] Figs. 39A to 39G show a BDD logic circuit using a charge recycle generator according to the 16th embodiment. In this case, when an AC-like power supply V1ac is used as a charge recycle generator for the BDD logic circuit shown in Fig. 36, a circuit obtained by connecting transmission gates 81 in series with each other is used instead of each of the inverters 25 to 27 in Figs. 38A to 38C. As shown in Figs. 39A and 39B, the circuit receives logic signals Ain and *Ain and generates AC voltage signals A and *A. As shown in Figs. 39C and 39D, the circuit receives logic signal Bin and *Bin and generates AC voltage signals B and *B. In addition, as shown in Figs. 39E and 39F, the circuit receives logic signals Cin and *Cin and generates AC voltage signals C and *C. These AC-like voltages A, *A, B, *B, C, and *C are input to the BDD logic circuit to perform logic processing.

[17th Embodiment]

[0086] Figs. 40A to 40D show a BDD logic circuit using a charge recycle generator according to the 17th embodiment, in which an AC-like voltage V1ac is used as an input voltage, and an AC-like voltage V2ac' is used as a power supply for the BDD logic circuit. This AC-like voltage V2ac' has a frequency twice that of the AC-like voltage V1ac. In addition, an n-channel MOSFET 28 having a switching function is connected between the BDD logic circuit and the AC-like voltage V2ac'. By supplying a clock signal ϕ (having the same frequency as that of the AC signal V1ac) to the gate of this n-channel MOSFET 28, as shown in Fig. 40D, the peaks of the AC-like voltage V2ac' are alternately extracted, thereby obtaining an AC-like voltage V2ac as a supply voltage.

[18th Embodiment]

[0087] Figs. 41A to 41G show a BDD logic circuit using a charge recycle generator according to the 18th embodiment, in which an AC-like voltage V1ac is used as an input voltage, and an AC-like voltage V2ac' is used for a charge recycle generator for the BDD logic circuit in Fig. 39G. Similar to the BDD logic circuit in Fig. 40D, this circuit uses an AC-like voltage V2ac as a supply voltage, which is obtained by alternately extracting the peaks of the AC-like voltage V2ac.

[0088] In the 18th embodiment and the 16th and 17th embodiments, as described above, the AC-like voltage need not be a sine-wave voltage. For example, a voltage having a trapezoidal or triangular waveform, an AC-like voltage based on a sine wave, or a voltage having a staircase waveform generated by the charge recycle generator 10B may be used. In addition, the relationship in timing between the AC-like voltages V1ac and V2ac can be arbitrarily set as long as the voltage V1ac rises earlier and falls later than the voltage V2ac.

[19th Embodiment]

[0089] Fig. 42A shows a BDD logic circuit according to the 19th embodiment. In this case, the charge recycle generator 10 of the BDD logic circuit shown in Fig. 28 is replaced with a charge no recycle generator 10'. The charge no recycle generator 10' is an AC-like power supply that does not recycle power. Fig. 42B shows the relationship between an AC-like power supply, the charge recycle generator 10, and the charge no recycle generator 10'.

[0090] Fig. 43 shows a circuit including the charge no recycle generator 10'. In this case, the rectangular wave output from an inverter 35 is integrated by a resistor 36 and a capacitor 37 to generate an AC-like voltage that moderately rises and falls. Even with such an AC-like power supply that does not recycle power, since adiabatic charging can be performed, unlike a power supply using a rectangular wave, the power consumption can be reduced to 1/2.

[0091] Note that as the elements of the logic circuits of the 12th to 19th embodiments described above, TFTs that are very suitable for adiabatic charging can be used, as described above. In addition, as shown in Fig. 25, these elements can be three-dimensionally integrated.

[0092] Furthermore, the logic circuits of the 12th to 19th embodiments described above can be equally applied to the IC card 60 according to the ninth embodiment in Fig. 24.

[20th Embodiment]

[0093] Fig. 44A shows a D latch logic circuit 90 as a logic circuit according to the 20th embodiment of the present invention. This circuit 90 is made up of two transmission gates 91 and 92 and cross-connected transmission gates 93 and 94 and inverters 95 and 96 which constitute a storage circuit.

[0094] In this case, as a supply voltage for each of the inverters 95 and 96, a voltage V3ac whose waveform moderately rises and falls as shown in Fig. 44B is used. As clock signals, a voltage V4ac, which rises after the

voltage V3ac falls, falls before the voltage V3ac rises, moderately rises and falls, and has a small duty, and an inverted voltage *V4ac are used, as shown in Fig. 44C. These voltages V3ac and V4ac are generated by using the oscillation type power supply circuit 10A in Fig. 2, which is a combination of an inductor and a capacitor, the staircase power supply circuit 10B in Figs. 3 and 8, which uses a plurality of capacitors to generate a staircase voltage by switching and charging/discharging the capacitors, a charge recycle generator such as a power supply circuit for generating a voltage by using one or a plurality of sine waves as shown in Figs. 4A to 4E, or an AC voltage obtained by an inductor for inducing the electromagnetic wave as described with reference to Fig. 24. In addition, waveforms (obtained by shifting the phase of V2ac from that of V1ac by 180°) similar to those shown in Figs. 21A to 21H can be used. Furthermore, a charge no recycle generator 10' (Figs. 22A and 23) can he used to generate the voltage V3ac and V4ac.

[0095] In this D latch logic circuit 90, while the voltage V4ac changes like Low → High → Low, the transmission gates 91 and 92 are temporarily turned on. At this time, the signals input to nodes 97 and 98 are transferred to nodes 99 and 100. When the voltage V4ac changes from High to Low, the transmission gates 91 and 92 are turned off, and the transmission gates 93 and 94 are turned on. As a result, the circuit is set in the storage mode. In the storage mode, since V3ac = 0 at first, even if the output signals from nodes 102 and 103 should be set at High, the potentials of the nodes have decreased to the voltage Vth (the threshold voltage of p-channel MOSFETs constituting the inverters 95 and 96). When the output signals are to be set at Low, the potentials of the nodes remain at 0 V.

[0096] When the voltage V3ac rises from 0 V to a supply voltage VDD, the potentials of the nodes 102 and 103 set at the threshold Vth slowly rise to the supply voltage VDD. When the voltage V3ac rises from VDD to 0 V afterward, the potentials of the nodes 102 and 103, which have been set at the supply voltage VDD, decrease to the threshold voltage Vth.

[0097] With this process, adiabatic charging is performed while the voltage V3ac rises from the threshold voltage Vth to the supply voltage VDD. If a charge recycle generator is used to generate the voltage V3ac, the charge is adiabatically recycled to the V3ac power supply side while the voltage V3ac drops from the supply voltage VDD to the threshold Vth. Such adiabatic charging and charge recycling are also executed at the transmission gate portion driven by the voltages V4ac and *V4ac in the same manner as described above.

[0098] As described above, in the conventional circuit (Fig. 66), the energy required for charging at the portion (transmission gates 91 to 94) driven by clock signals is $C_{TG}VDD^2$, whereas the energy required for charging in the circuit of the present invention is $C_{TG}VDD^2 \cdot 2\tau/T$, i.e., $2\tau/T$ times the energy in the conventional circuit. In this case, τ is the CR time constant of the circuit that is charged by the voltage V4ac, and T is the rise time (fall time) of the voltage V4ac. If, therefore, $\tau \ll T$ is set to perform charging/discharging sufficiently slowly, the energy can be sufficiently reduced, as shown in Fig. 45A. This allows a reduction in power consumption.

[0099] On the other hand, the charge energy in the portion associated with a storage circuit in the circuit of the present invention can be reduced from $1/2 \cdot C_{ME}VDD^2$ in the conventional circuit to $1/2 \cdot C_{ME}Vth^2$ because information is stored at Vth instead of VDD. Therefore, the energy required to charge/discharge this portion, which is $C_{ME}VDD^2$ in the conventional circuit as described above, becomes $C_{ME}Vth^2 + C_{ME}VDD^2 \cdot 2\tau/T$ (Fig. 45B). Note that T and τ are equal to those in the portion driven by clock signals.

[0100] As is obvious from the above description, the D latch logic circuit 90 allows a reduction in power consumption at both the transmission gate portion and the storage circuit portion.

[21st Embodiment]

[0101] Fig. 46 shows a D latch logic circuit according to the 21st embodiment of the present invention. In this circuit, the outputs of charge recycle type BDD logic circuits 110 and 120 are connected to the nodes 97 and 98 on the input side of the D latch logic circuit 90 in Fig. 44A.

[0102] The BDD logic circuits 110 and 120 are formed by combining n-channel MOSFETs 8 and p-channel MOSFETs 24. Signals A, B, and C to be applied to the gates of these MOSFETs are obtained by waveform conversion of input signals *a, *b, and *c, each having a rectangular wave, (inverting each signal and making the rising and falling slopes correspond to the rising and falling slopes of a voltage V3ac) by using inverters 131 to 133 to which the voltage V3ac is applied as supply voltage, as shown in Figs. 47A to 47C.

[0103] In this case, the p-channel MOSFETs 24 are connected between the outputs of the BDD logic circuits 110 and 120 and nodes 97 and 98 of the D latch logic circuit 90 in Fig. 46, and the inverted voltage *V5ac of a voltage V5ac having a waveform like the one shown in Fig. 48B is applied to the gate of each p-channel MOSFET 24. This voltage V5ac is also generated by the charge recycle generator or the charge no recycle generator described above. This voltage has a waveform that rises later and falls earlier than the voltage V3ac in Fig. 48A, and is also applied to one of the ending points of the BDD logic circuit 110 and the other ending point of the BDD logic circuit 120.

[0104] The operation of the BDD logic circuit shown in Fig. 46 will be described next.

[0105] First of all, the input signals A, B, and C are input to the BDD logic circuits 110 and 120 while changing to High and Low in synchronism with the voltage

V3ac. When the voltage V5ac rises, supply voltages are applied to the BDD logic circuits 110 and 120. In these circuits, logic processing (Exclusive OR (XOR) of the signals A, B, and C is performed in the BDD logic circuit 110, and Exclusive NOR (XNOR) of the signals A, B, and C is performed in the BDD logic circuit 120), and the logic processing results (Low-level or High-level signals) are transferred to the nodes 97 and 98 in synchronism with the leading edge of the voltage V5ac. Thereafter, the voltage V5ac falls. At this time, the signals are stored in the nodes 97 and 98. After the voltage V5ac falls, the voltage V3ac also falls. As a result, the input signals A, B, and C at the BDD logic circuits 110 and 120 fall.

[0106] When a voltage V4ac rises, transmission gates 91 and 92 are turned on, and the signals at the nodes 97 and 98 are transferred to nodes 99 and 100. Subsequently, the same operation as that of the circuit in Fig. 44A is performed in the D latch logic circuit 90 to output the inverted signals of the signals input to the nodes 97 and 98 to nodes 102 and 103 in synchronism with the voltage V3ac. A signal Q or an inverted signal *Q output from each of the nodes 102 and 103 can be used as an input signal to a D latch logic circuit on the next stage, which has the same arrangement as that described above, or as one of the input signals A, B, and C to the BDD logic circuits 110 and 120.

[0107] Figs. 48D to 48H explain a case wherein the outputs from the D latch logic circuit 90 are input to the BDD logic circuits 110 and 120.

[0108] As described above, in the logic circuit according to the 21st embodiment, logic processing is performed in the BDD logic circuits 110 and 120 by adiabatic charging and charge recycling, and the processing results are input to the D latch logic circuit 90 to be subjected to logic processing by adiabatic charging and charge recycling in the same manner as described above. Since the output signals can be sent to another circuit on the next stage or the input sides of the BDD logic circuits 110 and 120, low power consumption can be realized.

[22nd Embodiment]

[0109] Fig. 49A shows a D latch logic circuit according to the 22nd embodiment of the present invention, in which an inverter circuit 130 constituted by inverters 104 and 105 is connected to the nodes 102 and 103 of the D latch logic circuit 90 shown in Fig. 44A. Referring to Fig. 44A, reference numerals 106 and 107 denote output nodes.

[0110] As shown in Fig. 49C, a supply voltage V6ac applied to each of the inverters 104 and 105 moderately rises and falls, and rises later and falls earlier than voltage V3ac in Fig. 49B. This supply voltage V6ac is also generated by the charge recycle generator or charge no recycle generator described above.

[0111] Assume that a load having a very large capacitance is connected to the output nodes 102 and 103 of the D latch logic circuit 90 without the inverter circuit 130. In this case, even when the node 102 or 103 should be set at High by a signal transferred through a transmission gate 93 or 94 (since V3ac = 0 V in this case, the node is set at a threshold Vth as described above), the node instantaneously becomes 0 V. This potential is transferred to the load side. This may cause a data retention error.

[0112] In contrast to this, in this embodiment, the inverter circuit 130 is connected to the nodes 102 and 103, and a load having a large capacitance is connected to the nodes 106 and 107 of the inverter circuit 130. With this arrangement, since the nodes 106 and 107 do not directly receive the signals transferred through the transmission gates 93 and 94, data can be properly retained.

[23rd Embodiment]

[0113] Fig. 50 shows a D latch logic circuit according to the 23rd embodiment of the present invention, in which the BDD logic circuits 110 and 120 shown in Fig. 46 are connected to the nodes 97 and 98 on the input side of the D latch logic circuit 90 shown in Fig. 49A.

[0114] In this embodiment, voltages V3ac, V4ac, V5ac, and V6ac having timings and waveforms like those shown in Figs. 51A to 51D are used. Of these voltages, the voltage V5ac has a waveform that rises later and falls earlier than that of the voltage V6ac, and the voltage V6ac has a waveform that rises later and falls earlier than that of the voltage V3ac.

[0115] As a result, processing contents (XOR and XNOR) of signals A, B, and C input to the respective MOSFETs of the BDD logic circuits 110 and 120 are output to nodes 97 and 98 in synchronism with the voltage V5ac, and then transferred to nodes 99 and 100 in synchronism with the voltage V4ac, the nodes 102 and 103 in synchronism with the voltage V3ac, and nodes 106 and 107 in synchronism with the voltage V6ac. The signals obtained at the nodes 106 and 107 can be used as input signals to the BDD logic circuits 110 and 120.

[24th Embodiment]

[0116] Fig. 52A shows a D latch logic circuit 90A according to the 24th embodiment of the present invention, in which the transmission gates 91 and 92 of the D latch logic circuit 90 in Fig. 44A are replaced with n-channel MOSFETs 8. In this case, a non-inverted voltage V4ac is applied to the gate of each n-channel MOSFET 8. Note that the transmission gates 91 and 92 may be replaced with p-channel MOSFETs 24 as in a D latch logic circuit 90B in Fig. 52B. In this case, an inverted voltage *V4ac of the voltage V4ac is applied to the gate of each p-channel MOSFET 24.

[0117] By using a single MOSFET as transmission gate in this manner, the number of transistors can be

decreased.

[25th Embodiment]

[0118] Figs. 53A to 53C show a logic circuit according to the 25th embodiment. In a 2-bit adder 140 in Fig. 53C, a circuit portion for outputting a sum S1 and its inverted signal *S1 upon reception of two data bits A1 and A0, two data bits B1 and B0, and one carry bit C0 is constituted by a PMOS latch logic circuit 140A and a BDD logic circuit 140B, as shown in Fig. 53B.

[0119] Two p-channel MOSFETs 24 are used for the PMOS latch logic circuit 140A, but no transmission gate and inverter are used. A voltage V3ac is connected to the source of the PMOS latch logic circuit 140A. The BDD logic circuit 140B is obtained by implementing the BDD graph shown in Fig. 53A using a plurality of n-channel MOSFETs 8. The output signal S1 and the inverted signal *S1 thereof output from the BDD logic circuit 140B and appearing at nodes 141 and 142 are held in the PMOS latch logic circuit 140A and transferred to the next stage (not shown). The beginning point of the BDD logic circuit 140B is grounded.

[0120] In this embodiment, after the input signals A1, A0, B1, B0, and C0 are input, the voltage V3ac of the power supply rises, thereby performing logic processing. Thereafter, the voltage V3ac falls, and the input signals A1, A0, B1, B0, and C0 fall. When voltage V3ac = 0, the High-side potentials of the output nodes 141 and 142 of the PMOS latch logic circuit 140A have dropped to a threshold voltage Vth of each p-channel MOSFET. When the voltage V3ac rises to a supply voltage VDD, adiabatic charging is performed. When the voltage V3ac drops to 0 V afterwards, charge recycling is performed. This allows a reduction in power consumption.

[0121] By combining the PMOS latch logic circuit and the BDD logic circuit, therefore, "High" of the output signal S1 and the inverted signal *S1 can be set to the peak value of V3ac, and "Low" of these signals can be set to 0 V, thus setting the voltage values of the signals to the proper values. In addition, the use of a BDD logic circuit allows a decrease in the number of transistors and efficient circuit integration. Furthermore, even a large-scale BDD logic circuit can be easily designed and formed by computer-aided designing.

[0122] Obviously, in addition to the above gate input/supply voltage control method, control based on a four-phase clock scheme can be performed (reference 3: Y. Moon and D. K. Jeong "An Efficient Change Recovery Logic Circuit" IEEE Journal of Solid-state circuits, Vol. 31, NO. 4 April 1996).

[26th Embodiment]

[0123] Figs. 54A to 54C show a logic circuit according to the 26th embodiment. In a 2-bit adder 140 (identical to the circuit in Fig. 53C) in Fig. 54C, a circuit portion for outputting a carry bit C2 and its inverted signal upon reception of two data bits A1 and A0, two data bits B1 and B0, and one carry bit C0 is constituted by a PMOS latch logic circuit 140C and a BDD logic circuit 140D, as shown in Fig. 54B.

[0124] Similar to the PMOS latch logic circuit 140A, the PMOS latch logic circuit 140C uses two p-channel MOSFETs 24. A voltage V3ac is connected to the source of the PMOS latch logic circuit 140C. The BDD logic circuit 140D is obtained by implementing the BDD graph shown in Fig. 54A using a plurality of n-channel MOSFETs 8. The output signal C2 and an inverted signal *C2 thereof output from the BDD logic circuit 140D and appearing at nodes 143 and 144 are latched by the PMOS latch logic circuit 140C and transferred to the next stage (not shown).

[0125] The operation of this embodiment is almost the same as that of the circuit shown in Fig. 53B. When voltage V3ac = 0, the High-side potentials of the output nodes 143 and 144 have dropped to a threshold voltage Vth of each p-channel MOSFET. When the voltage V3ac rises to VDD, adiabatic charging is performed. When the voltage V3ac drops to 0 V afterward, charge recycling is performed. This allows a reduction in power consumption.

[27th Embodiment]

[0126] Fig. 55 shows a logic circuit according to the 27th embodiment. This logic circuit is a flip-flop circuit constituted by an NMOS BDD logic circuit 140B or 140D and inverters 140G1 and 140G2.

[0127] Figs. 56A and 56B show examples of how a flip-flop circuit 140G constituted by the inverters 140G1 and 140G2 and the NMOS BDD logic circuit 140B or 140D are connected to each other.

[28th Embodiment]

[0128] Fig. 57A shows a logic circuit according to the 28th embodiment, which is a modification of the logic circuit in Fig. 53B. In this modification, an NMOS latch logic circuit 140A' is constituted by n-channel MOSFETs 8 with their sources being grounded, and a BDD logic circuit 140B' is constituted by p-channel MOSFETs 24 alone with a voltage V3ac being connected to the beginning point of the BDD logic circuit 140B'.

[0129] In this case, the logic processing results obtained by the BDD logic circuit 140B' appear at nodes 141 and 142 when the voltage V3ac rises. The results are then latched by the NMOS latch logic circuit 140A'. That is, adiabatic charging and charge recycling are also performed in this logic circuit.

[29th Embodiment]

[0130] Fig. 57B shows a logic circuit according to the 29th embodiment, which is a modification of the circuit in Fig. 54B. In this modification, an NMOS latch logic cir-

cuit 140C' is constituted by n-channel MOSFETs 8 with their sources being grounded, and a BDD logic circuit 140D' is constituted by p-channel MOSFETs 24 alone with a voltage V3ac being connected to the beginning point of the BDD logic circuit 140D'.

[0131] In this case as well, when the voltage V3ac rises, the logic processing results obtained by the BDD logic circuit 140D' appear at nodes 143 and 144, thus performing adiabatic charging and charge recycling.

[30th Embodiment]

[0132] Fig. 58A shows a logic circuit according to the 30th embodiment, which is a modification of the circuit in Fig. 53B. In this modification, a voltage V3ac is connected to the source of each p-channel MOSFET 24 of a PMOS latch logic circuit 140A, and the same voltage V3ac is also connected to the beginning point of a BDD logic circuit 140B.

[0133] In this case, one of nodes 141 and 142 at which a Low-level signal appears is set in a floating state, but has a potential close to the ground potential instead of a high impedance. This was confirmed by a simulation. On the side where a High-level signal appears, adiabatic charging and charge recycling are performed.

[31st Embodiment]

[0134] Fig. 58B shows a logic circuit according to the 31st embodiment, which is a modification of the circuit in Fig. 54B. In this modification, a voltage V3ac is connected to the source of each p-channel MOSFET 24 of a PMOS latch logic circuit 140C, and the same voltage V3ac is also connected to the beginning point of a BDD logic circuit 140D.

[0135] In this case as well, one of nodes 143 and 144 at which a Low-level signal appears is set in a floating state, but has a potential close to the ground potential instead of a high impedance. This was confirmed by a simulation. On the side where a High-level signal appears, adiabatic charging and charge recycling are performed.

[32nd Embodiment]

[0136] Figs. 59A and 59B show logic circuits according to the 32nd embodiment, in which each of BDD logic circuits 140E and 140F connected to a PMOS latch logic circuit 140C and an NMOS latch logic circuit 140A' is made up of a mixture of n-channel MOSFETs and p-channel MOSFETs. With this arrangement, an inverter connected to each input gate can be omitted.

[0137] Note that TFTs that are very suitable for adiabatic charging as described with reference to Fig. 25 and can be used as the elements of the logic circuits of the 20th to 32nd embodiments.

[33rd Embodiment]

[0138] In a conventional CMOS logic circuit, to prevent disconnection of wires due to electromigration, the current density is set to a given upper limit value J_0 or less. In general, a life τ of a wire influenced by electromigration can be represented as:

$$\tau = KST/\{J^2 Dexp(-\Delta E/kT)\} \quad (1)$$

where K is the proportional constant, S is the cross-sectional area of the wire, T is the absolute temperature, J is the current density, D is the diffusion coefficient of an aluminum atom, and k is the Boltzmann's constant (reference 4: "CMOS ULSI Design", supervised by Sadao Sugano, edited by Tetsuya Iizuka, published by Baihuukan, 1996, pp. 87 - 88).

[0139] Obviously, as the wire width decreases and the current density J increases, the time τ that elapses before disconnection shortens. In a CMOS logic circuit, therefore, the cross-sectional area of a wire has its lower limit value. In other words, the current density has its upper limit value.

[0140] In an actual CMOS logic LSI, for example, when the supply voltage is set to 2 V, a current of about 8 mA flows in a signal line, and the current density is about 2.7×10^6 A/cm^2. In this case, the cross-sectional area of the signal line is about $(0.55\ \mu m)^2 = 0.30\ \mu m^2$ (see Figs. 60B and 67).

[0141] In a BDD logic circuit, a D latch logic circuit, or the like using the above adiabatic charging logic, since charging/discharging is performed adiabatically, the density of current flowing in a metal wire or transistor is very low. The electromigration effect on each wire is therefore small. This allows the cross-sectional area of a wire to be smaller than the above value, $(0.55\ \mu m)^2 = 0.30\ \mu m^2$, in the conventional CMOS logic LSI.

[0142] According to the 33rd embodiment, therefore, in a logic circuit based on adiabatic charging logic, reductions in wire cross-sectional area and power consumption are achieved while the life of each wire influenced by electromigration is set to be substantially equal to that in the conventional CMOS logic circuit.

[0143] Since the current I is represented as I = SJ in equation (1) above,

$$\tau = KTS^3/\{I^2 Dexp(-\Delta E/kT)\} \quad (2)$$

As is obvious from this equation, the life of each wire influenced by electromigration is proportional to S^3/I^2.

[0144] Letting τ_0, S_0, and I_0 be the average life of wires, the wire cross-sectional area, and the current flowing in each wire, respectively, in a CMOS logic circuit, the relationship between these values is represented by

$$\tau_0 = aS_0^3/I_0^2 \quad (3)$$

where a is a proportional constant.

[0145] Letting τ, S, and I be the average life of wires, the wire cross-sectional area, and the current flowing in each wire, respectively, in a logic circuit that performs adiabatic charging, the relationship between these values is represented by

$$\tau = aS^3/I^2 \quad (4)$$

Therefore,

$$\tau/\tau_0 = (S/S_0)^3(I_0/I)^2 \quad (5)$$

If the lives of wires in the two circuits are equal, i.e., $\tau_0 = \tau$,

$$S = S_0(I/I_0)^{2/3} \quad (6)$$

[0146] In the case of adiabatic charging, since the circuit operates slowly, the current value can be decreased up to, for example, 1/1000 of that in the CMOS logic circuit. If, therefore, the cross-sectional area is decreased to 1/100 when the current value becomes 1/1000 of that in the CMOS logic circuit, the lives of wires in the two circuits are equal.

[0147] For example, as shown in Fig. 60A, therefore, an ultra-thin wire having a width of 0.15 μm and a thickness of 0.02 μm (cross-sectional area: 0.0030 μm^2) can be used. Even a wire with a thickness of 0.2 μm (cross-sectional area = 0.030 μm^2) has a cross-sectional area 1/10 of that (0.30 μm^2) of a general wire, and hence a sufficient effect can be expected.

[0148] As is obvious from the above description, the wire capacitance can be reduced to 1/10 to 1/100. As shown in Fig. 60C, the power consumption in charging can be reduced to 1/10 to 1/100.

[0149] Furthermore, since no large current driving ability is required in each transistor as well as in each wire, the transistor width (channel width) can be reduced to about 0.1 μm, which is about 1/100 of the transistor width (about 10 μm) in the conventional circuit. This allows a reduction in the capacitance of each transistor.

[34th Embodiment]

[0150] When electrical signals are to be transferred on the basis of adiabatic charging logic, a reduction in wire cross-sectional area can be attained because the transfer operation can be performed moderately and slowly. This operation will be described next.

[0151] Assume that a cross-sectional area A of a wire is decreased to 1/k times. In this case, a resistance R increases k times. In general, the capacitance of the wire is sufficiently smaller than that of the load of a gate on the next stage. A capacitance C can therefore be regarded as constant. Consequently, the following equation can be approximately formulated:

$$A \times CR = \text{constant} \quad (7)$$

[0152] Letting S_0 be the cross-sectional area of a wire in a CMOS logic circuit, and S be the cross-sectional area of a wire in an adiabatic charging logic circuit, the following equation is formulated:

$$S_0(CR)_{CMOS} = S(CR)_{adiabatic} \quad (8)$$

[0153] In adiabatic charging, electrical signals can be transferred slowly, and hence $10 \times (CR)_{CMOS} \leq (CR)_{adiabatic}$ can be set. Therefore,

$$S = S_0(CR)_{CMOS}/(CR)_{adiabatic} \leq 1/10 \times S_0 \quad (9)$$

[0154] In addition, since a time T required to rise the power supply for the adiabatic charging circuit must be larger than the CR time constant of the adiabatic charging circuit,

$$(CR)_{adiabatic} \leq T \quad (10)$$

Therefore,

$$S_0(CR)_{CMOS} = S(CR)_{adiabatic} \leq ST \quad (11)$$

[0155] If $(CR)_{CMOS} = \tau$, then

$$\tau/T \times S_0 \leq S \quad (12)$$

From mathematical expressions (9) and (12),

$$\tau/T \times S_0 \leq S \leq 1/10 \times S_0 \quad (13)$$

[0156] Assume that the cross-sectional area of a wire 400 formed in the CMOS logic circuit shown in Fig. 67 and having a signal wire width W_0 of 550 nm (0.55 μm) and a signal wire thickness H_0 of 550 nm (0.55 μm) is to be decreased. In this case, if τ/T is set to 1/100, a cross-sectional area S falls within the range of $0.003\ \mu m^2 \leq S \leq 0.03\ \mu m^2$.

[0157] As is obvious from the above description, an ultra-thin wire like the one shown in Fig. 60A can be used.

[35th Embodiment]

[0158] Figs. 61A to 61C explain the 35th embodiment of the present invention. The cross-sectional area of each signal wire in the CMOS logic circuit shown in Fig. 67 can be reduced to 1/10 to 1/100, as described above. The cross-sectional areas of power and ground lines in this logic circuit can also be reduced.

[0159] More specifically, a cross-sectional area S_0 of a power or ground line 410 in Fig. 61A which is formed in a logic circuit and has a width of 30 μm and a thickness of 3 μm can be reduced to 1/10, i.e., $(1/10 \times S_0)$, according to the adiabatic charging logic, as shown in

Fig. 61B. In addition, as shown in Fig. 61C, the cross-sectional area S_0 can be reduced to 1/100, i.e., (1/100 x S_0).

[0160] According to the adiabatic charging logic, therefore, the cross-sectional areas of the power and ground lines in the logic circuit, as well as the signal lines, can be reduced to 1/10 to 1/100.

[0161] Obviously, in the 33rd to 35th embodiments, the cross-sectional areas of the signal, power, and ground lines can be reduced up to 1/1000 by performing adiabatic charging more slowly.

[0162] As described above, according to the adiabatic charging logic, the cross-sectional area of each wire can be reduced, and efficient logic processing can be realized by transfer of a small number of electrons. This can greatly reduce the energy per logic operation as compared with the conventional CMOS logic circuit.

[0163] As has been described above, according to the present invention, in a BDD logic circuit, a D latch logic circuit, or the like having several hundred or several thousand gates, adiabatic charging and charge recycling can be realized very easily. This can attain reductions in power consumption and circuit size as compared with the conventional CMOS logic circuit and D latch logic circuit.

[0164] In addition, according to the present invention, since charging/discharging is performed adiabatically, the density of a current flowing in each metal wire and each transistor is very low. For this reason, the electromigration effect on each wire is small, and the cross-sectional area of each wire can be greatly decreased as compared with the cross-sectional area of each wire in a CMOS logic circuit. This allows a reduction in wire capacitance.

[0165] As described above, according to the present invention, efficient logic processing can be realized by transfer of a smaller number of electrons, and hence the energy per logic operation can be greatly reduced as compared with the conventional CMOS logic circuit.

Claims

1. An adiabatic charging logic circuit characterized by comprising:

   a logic circuit (30A, 30B, 90) constituted by a plurality of logic elements; and
   a power supply section (10, 10A, 10B, 10') for supplying power to said logic circuit to cause said logic circuit to perform logic processing after an input signal is supplied to a gate of each of the logic elements, and stopping supply of the power before a new input signal is supplied to the gate of each of the logic elements after completion of the logic processing.

2. A circuit according to claim 1, wherein said logic circuit is a BDD logic circuit (30A, 30B) formed on the basis of a binary decision diagram having beginning points (1, 2), ending points (3, 4), nodes (5) arranged between the beginning points and the ending points, and branches (6, 7) arranged at the nodes and connecting the nodes, the plurality of logic elements are arranged in correspondence with the branches of the binary decision diagram, and said power supply section is connected to a portion corresponding to one of the beginning and ending points of the binary decision diagram.

3. A circuit according to claim 2, wherein said BDD logic circuit is a BDD logic circuit (30A) in which a portion corresponding to one ending point of the binary decision diagram is grounded, said power supply section is connected to a portion corresponding to the other ending point of the binary decision diagram, and output signals are extracted from portions corresponding to the beginning points of the binary decision diagram when a supply voltage is applied from said power supply section after an input signal is supplied to the gate of each of the logic elements.

4. A circuit according to claim 3, wherein the binary decision diagram has no single but plural beginning points by combining a plurality of different binary decision diagrams.

5. A circuit according to claim 2, wherein said BDD logic circuit is a BDD logic circuit (30B) in which said power supply section is connected to the beginning point of the binary decision diagram, and an output signal and an inverted output signal are respectively extracted from portions corresponding to one ending point and the other ending point of the binary decision diagram when a supply voltage is applied from said power supply section after an input signal is supplied to the gate of each of the logic elements.

6. A circuit according to claim 2, wherein said circuit further comprises a plurality of BDD logic circuits (30_1 - 30_n), and said power supply section applies a first voltage having a high frequency to a BDD logic circuit, of said plurality of BDD logic circuits, which performs logic processing at a high speed, a second voltage having a low frequency to a BDD logic circuit which performs logic processing at low speed, and third voltages having the same frequency and the same phase to BDD logic circuits which perform logic processing in phase at the same speed.

7. A circuit according to claim 2, wherein the plurality of logic elements comprise complementary logic elements (8, 24), and one of non-inverted and inverted signals of the input signal is supplied to a

gate of each of the logic elements.

8. A circuit according to claim 2, wherein the logic element comprises two complementary logic elements (81) connected in parallel with each other, and eliminates a change in output voltage based on a threshold voltage.

9. A circuit according to claim 2, wherein one of a power supply of said power supply section and a power supply that rises earlier and falls later than the power supply of said power supply section is used as a power supply for an input signal to be applied to the gate of the logic element, thereby adiabatically charging the gate.

10. A circuit according to claim 1, wherein said logic circuit is a D latch logic circuit (90) including a signal receiving circuit constituted by a first transmission gate pair (91, 92), and a storage circuit having a first inverter pair (95, 96) for inverting output signals from the first transmission gate pair and a second transmission gate pair (93, 94) which are turned on to input the output signals from the first inverter pair to the inverters on opposite sides when the first transmission gate pair are turned off, uses a first voltage that moderately rises and falls as a supply voltage from said power supply section to the first inverter pair, and uses a second voltage, which rises after the first voltage falls and falls before the first voltage rises, and an inverted voltage thereof as gate voltages to be applied to the first and second transmission gate pairs.

11. A circuit according to claim 10, wherein a second inverter pair (104, 105) are connected to output sides of the first inverter pair, and a supply voltage to the second inverter pair is a third voltage that rises later and falls earlier than the first voltage.

12. A circuit according to claim 10, wherein the first transmission gate pair are a transmission gate pair comprising one of a p-channel MOSFET and an n-channel MOSFET.

13. A circuit according to claim 10, wherein said logic circuit is a BDD logic circuit formed on the basis of a binary decision diagram having beginning points (1, 2), ending points (3, 4), nodes (5) arranged between the beginning points and the ending points, and branches (6, 7) arranged at the nodes and connecting the nodes, the plurality of logic elements are arranged in correspondence with the branches of the binary decision diagram, and said power supply section is connected to a portion corresponding to one of the beginning and ending points of the binary decision diagram, and

input sides of the first transmission gate pair are connected to output sides of said two BDD logic circuits, and a supply voltage applied to each BDD logic circuit is a fourth voltage whose waveform rises later and falls earlier than a waveform of the first voltage.

14. A circuit according to claim 13, wherein output signals from said D latch logic circuit are used as input signals to said two BDD logic circuits.

15. A circuit according to claim 1, wherein said logic circuit comprises: a BDD logic circuit (140B, 140D) formed on the basis of a binary decision diagram having beginning points (1, 2), ending points (3, 4), nodes (5) arranged between the beginning points and the ending points, and branches (6, 7) arranged at the nodes and connecting the nodes, the plurality of logic elements being arranged in correspondence with the branches of the binary decision diagram, and said BDD logic circuit having a portion corresponding to the beginning point of the binary decision diagram and grounded; and one of a flip-flop circuit (140G) and a PMOS latch logic circuit (140A, 140C), each having an output and a gate connected to each other, the gate being connected to an output of said BDD logic circuit, and said power supply section having a power supply connected thereto.

16. A circuit according to claim 1, wherein said logic circuit comprises: a BDD logic circuit (140B', 140D') formed on the basis of a binary decision diagram having beginning points (1, 2), ending points (3, 4), nodes (5) arranged between the beginning points and the ending points, and branches (6, 7) arranged at the nodes and connecting the nodes, the plurality of logic elements being arranged in correspondence with the branches of the binary decision diagram, and said BDD logic circuit having a portion corresponding to the beginning point of the binary decision diagram and connected to said power supply section; and an NMOS latch circuit (140A', 140C') having an output and a gate connected to each other, the gate being connected to an output of said BDD logic circuit, and said NMOS latch circuit having a source grounded.

17. A circuit according to claim 1, wherein said logic circuit comprises: a BDD logic circuit (140B, 140D) formed on the basis of a binary decision diagram having beginning points (1, 2), ending points (3, 4), nodes (5) arranged between the beginning points and the ending points, and branches (6, 7) arranged at the nodes and connecting the nodes, the plurality of logic elements being arranged in correspondence with the branches of the binary decision diagram, and said BDD logic circuit having a portion corresponding to the beginning point of the

binary decision diagram and connected to said power supply section; and a PMOS latch logic circuit (140A, 140C) having an output and a gate connected to each other, the gate being connected to an output of said BDD logic circuit, and said power supply section having a power supply connected thereto.

18. A circuit according to claim 1, wherein said power supply section is a charge recycle generator (10, 10A, 10B).

19. A circuit according to claim 1, wherein said power supply section is a charge-no-recycle generator (10').

20. A circuit according to claim 1, wherein said power supply section supplies AC power obtained from an inductor (62) for inducing a radio electromagnetic wave as power to said logic circuit.

21. A circuit according to claim 1, wherein a TFT is used as the logic element.

22. A circuit according to claim 1, wherein the logic elements are three-dimensionally integrated.

23. A circuit according to claim 1, wherein a cross-sectional area S of a signal wire of said logic circuit, which is equal to a cross-sectional area S_0 of a wire in a CMOS logic circuit, is represented by

$$(I/I_0)^{2/3} \times S_0 \leq S \leq 1/10 \times S_0$$

where I_0 is an upper limit value of a wire current which is obtained from the cross-sectional area of the wire in said logic circuit on the basis of a life influenced by electromigration, and I is a value of a current flowing in said logic circuit during adiabatic charging logic operation.

24. A circuit according to claim 1, wherein a cross-sectional area S of a signal wire of said logic circuit, which is equal to a cross-sectional area S_0 of a wire in a CMOS logic circuit, is represented by

$$\tau/T \times S_0 \leq S \leq 1/10 \times S_0$$

where τ is a CR time constant of the signal wire in said logic circuit, and T is a time required for a supply voltage to reach a peak value after power is supplied to said logic circuit by adiabatic charging logic.

25. A circuit according to claim 23 or 24, wherein when the cross-sectional area S_0 of the signal wire is 0.3 μm^2, the cross-sectional area S falls within a range of 0.003 μm^2 to 0.03 μm^2.

26. A circuit according to claim 23 or 24, wherein cross-sectional areas of power and ground lines of said logic circuit are decreased.

27. A circuit according to claim 26, wherein the cross-sectional areas of the power and ground lines of said logic circuit are decreased to fall within a range of 1/10 to 1/100.

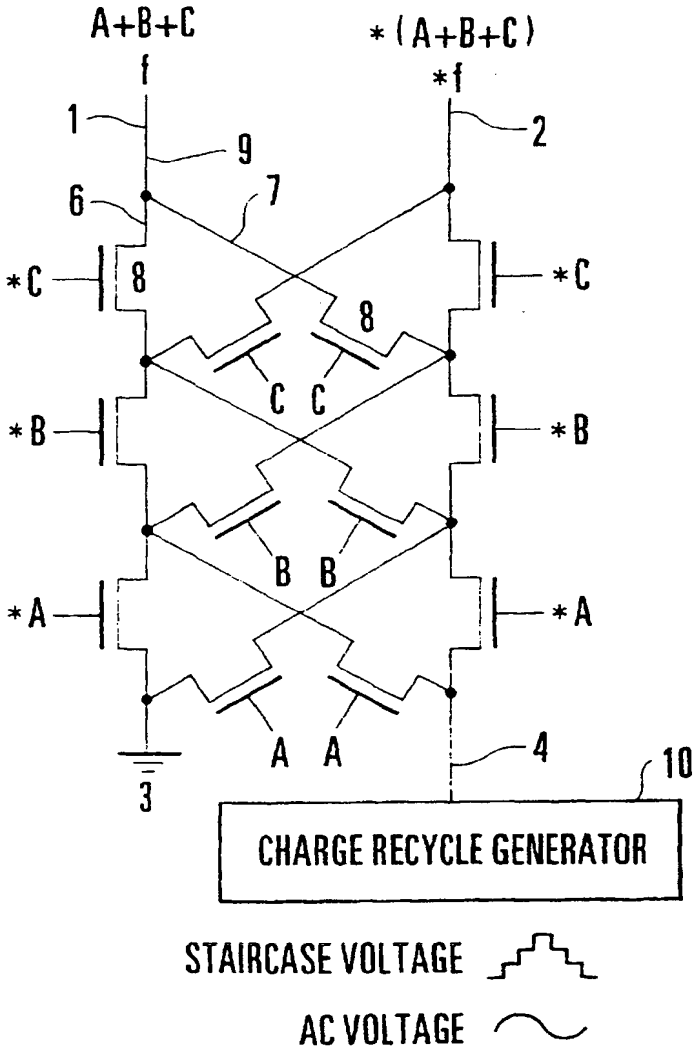


FIG. 1

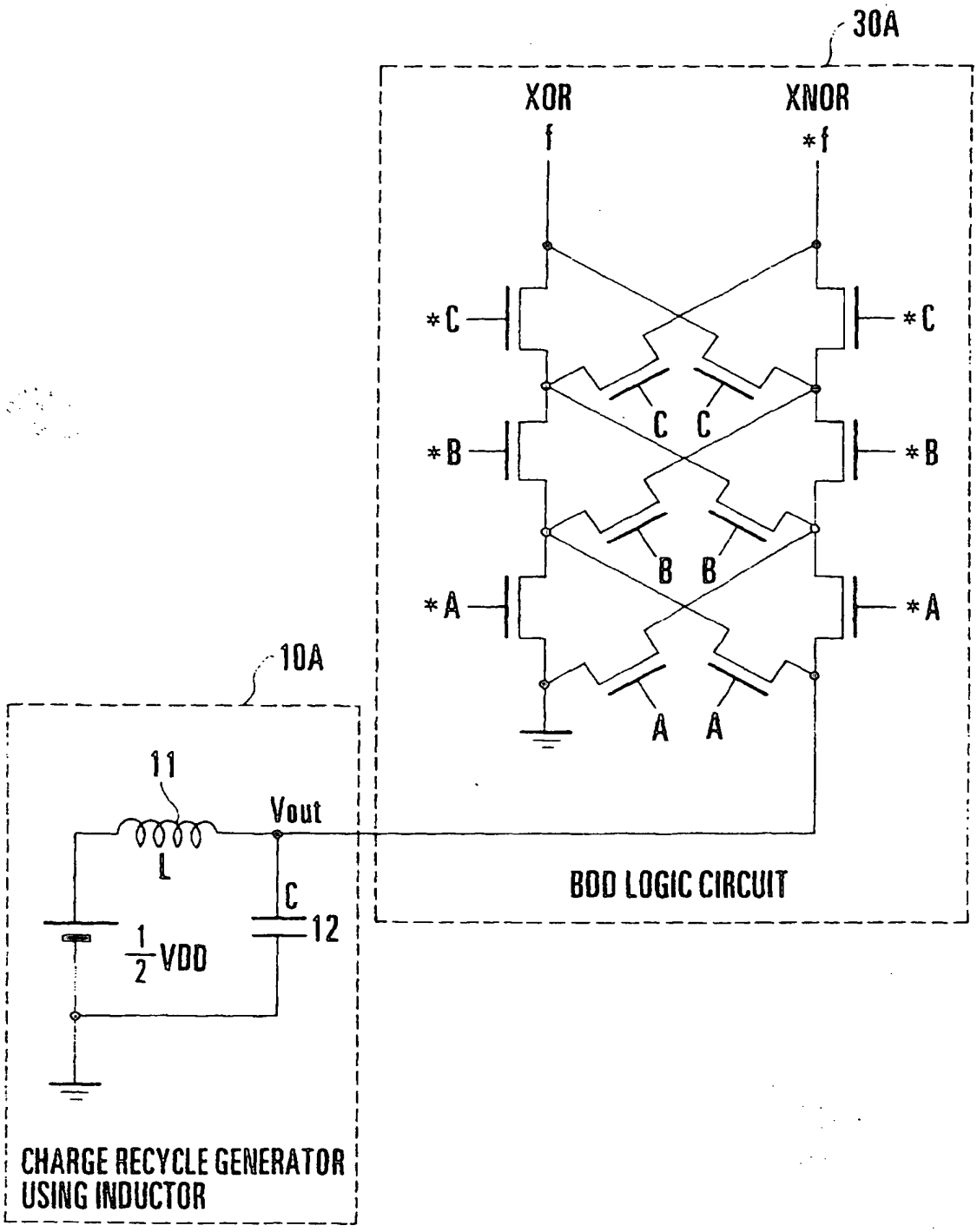


FIG. 2

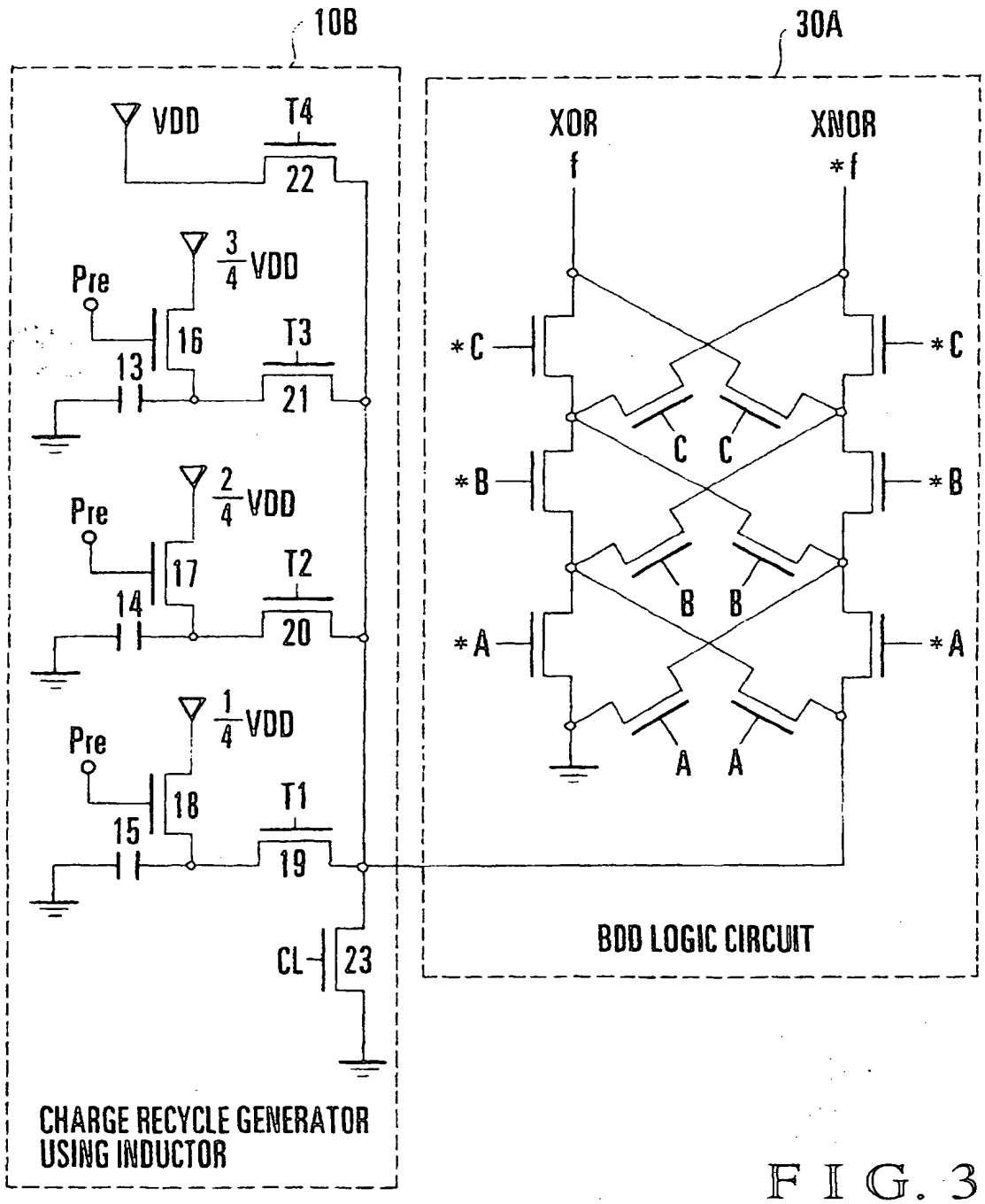


FIG. 3

FIG. 4A

FIG. 4B

FIG. 4C

FIG. 4D

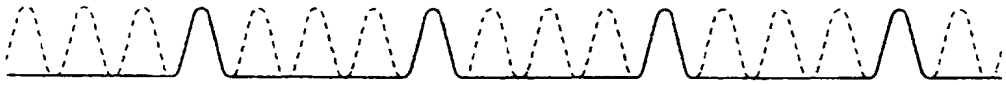
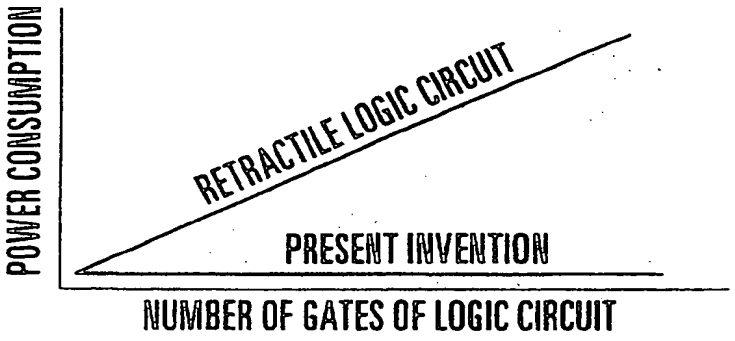


FIG. 4E

FIG. 4F



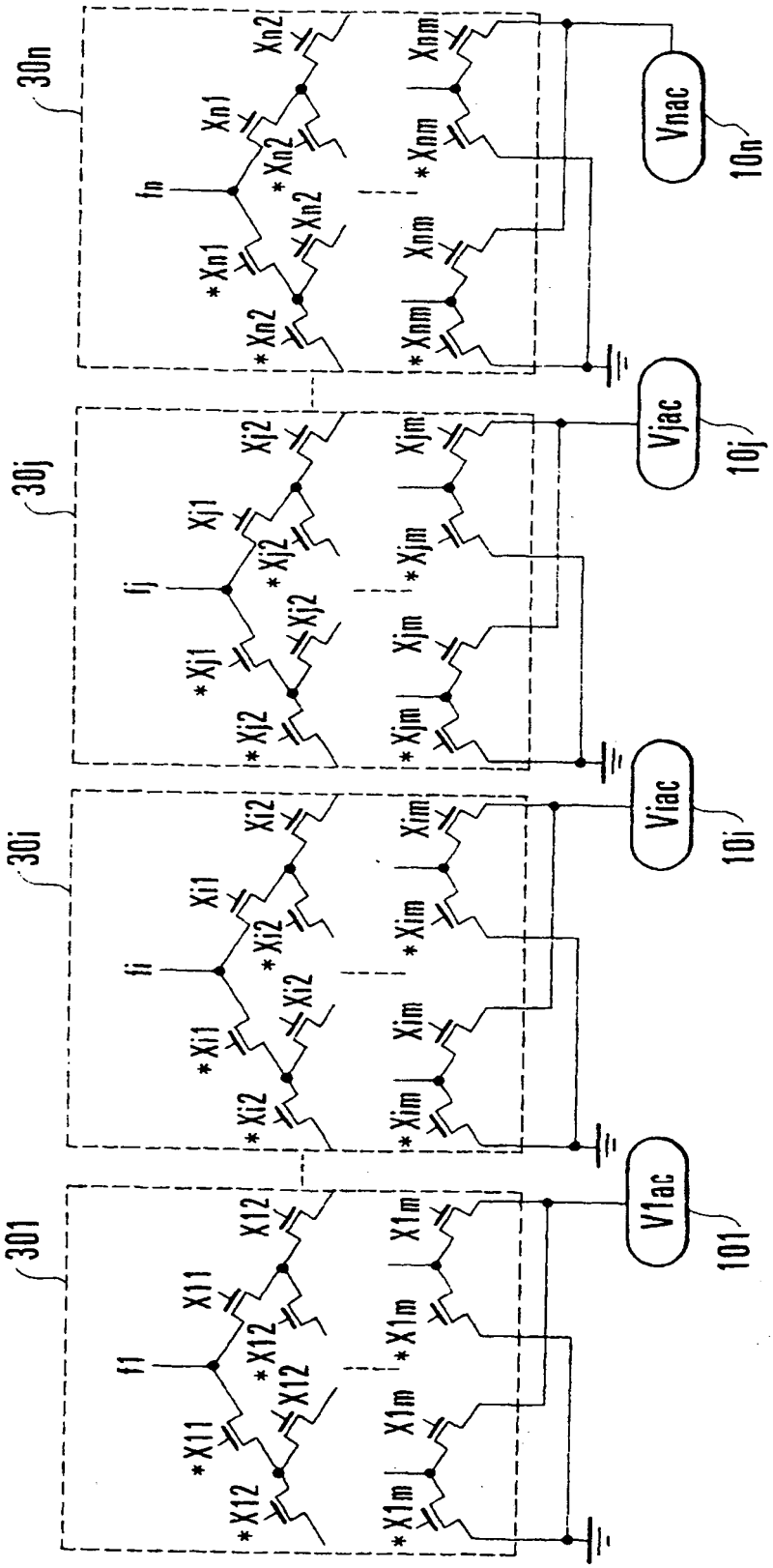


FIG. 5

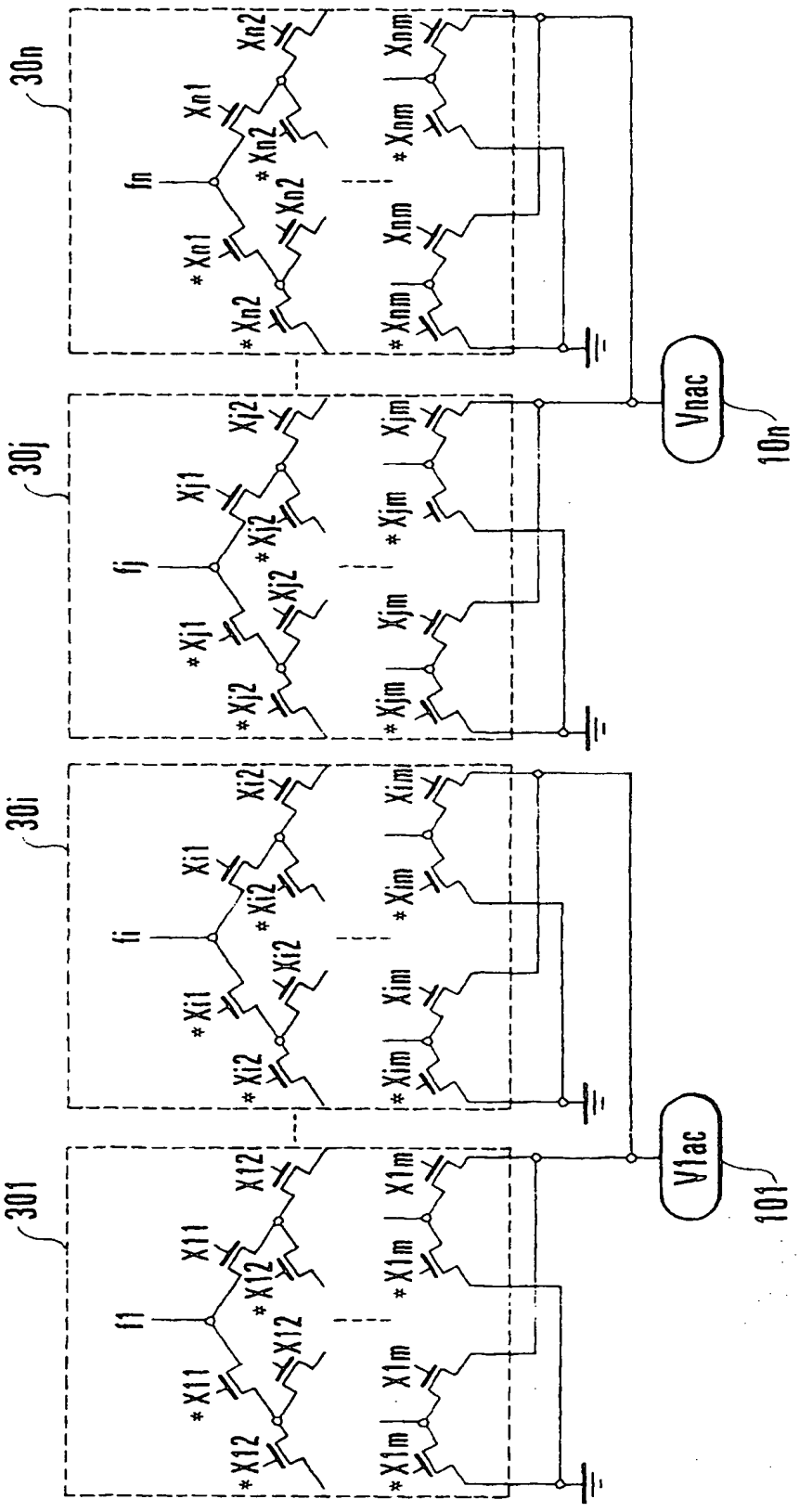


FIG. 6

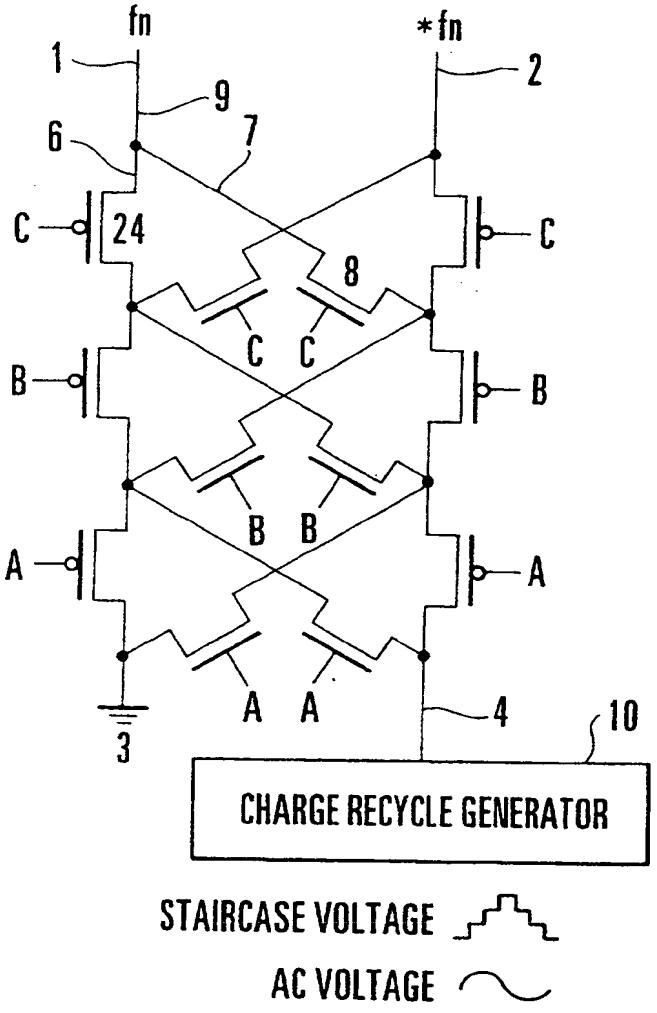


FIG. 7

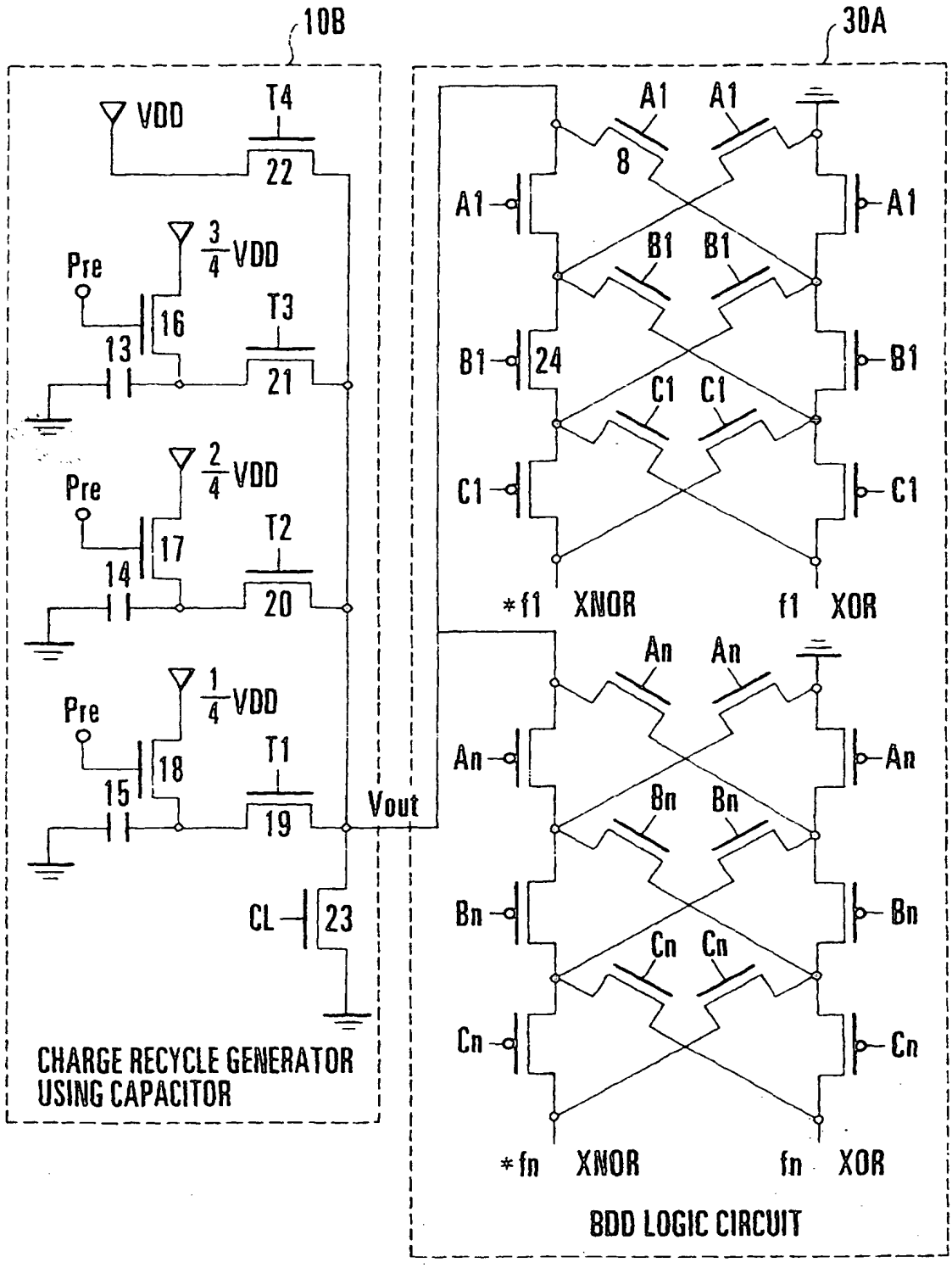


FIG. 8

FIG. 9A

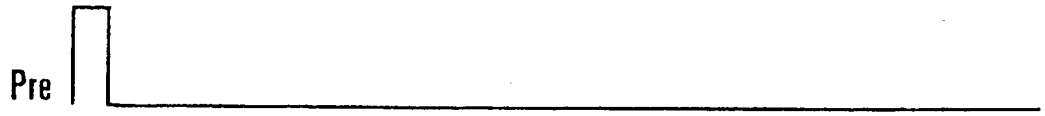


FIG. 9B

FIG. 9C

FIG. 9D

FIG. 9E

FIG. 9F

FIG. 9G

FIG. 9H

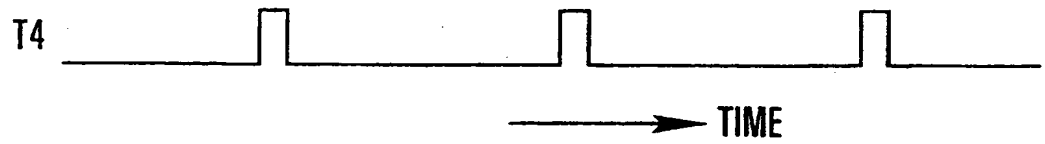


FIG. 10A

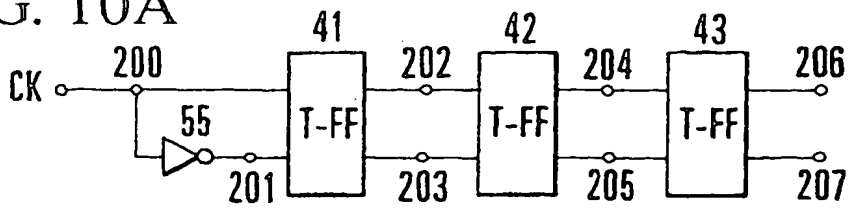


FIG. 10B

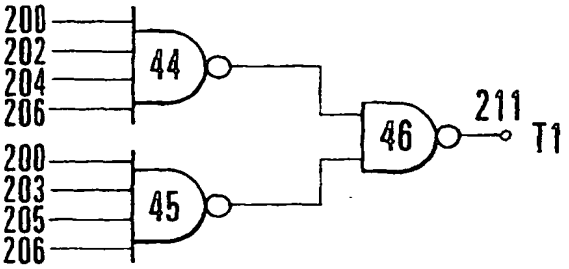


FIG. 10C

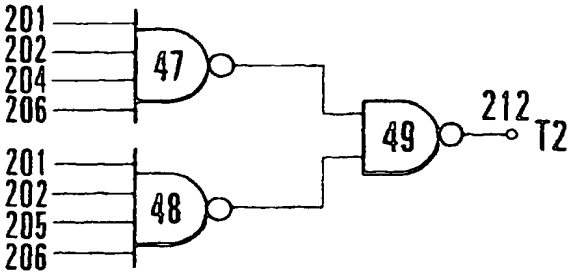


FIG. 10D

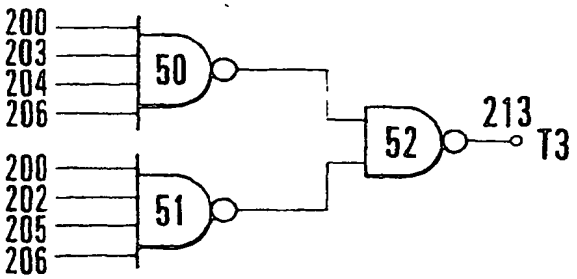


FIG. 10E

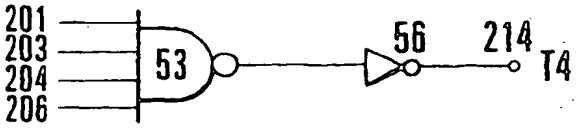
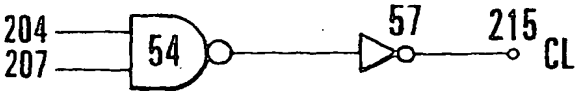


FIG. 10F



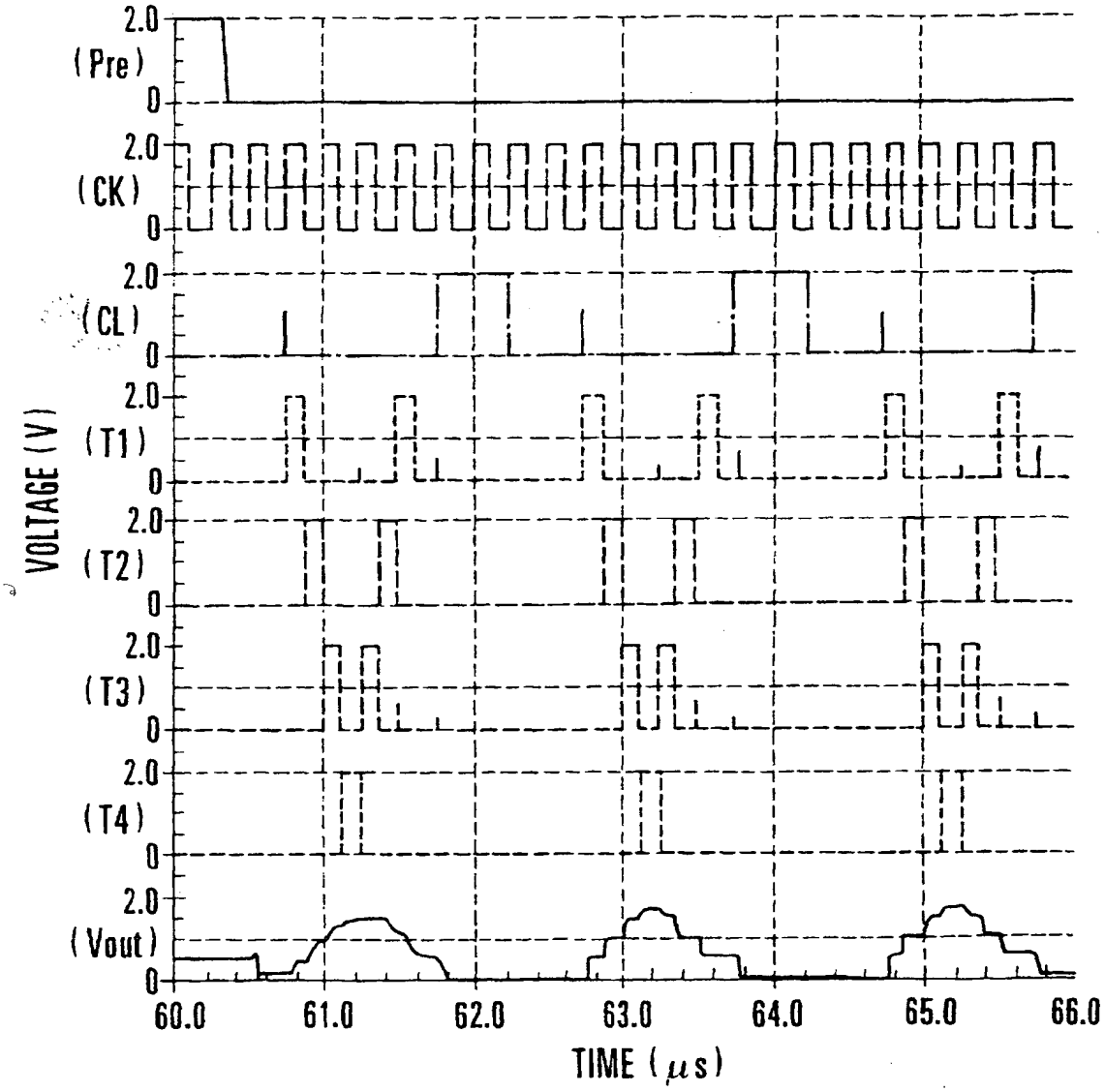


FIG. 11

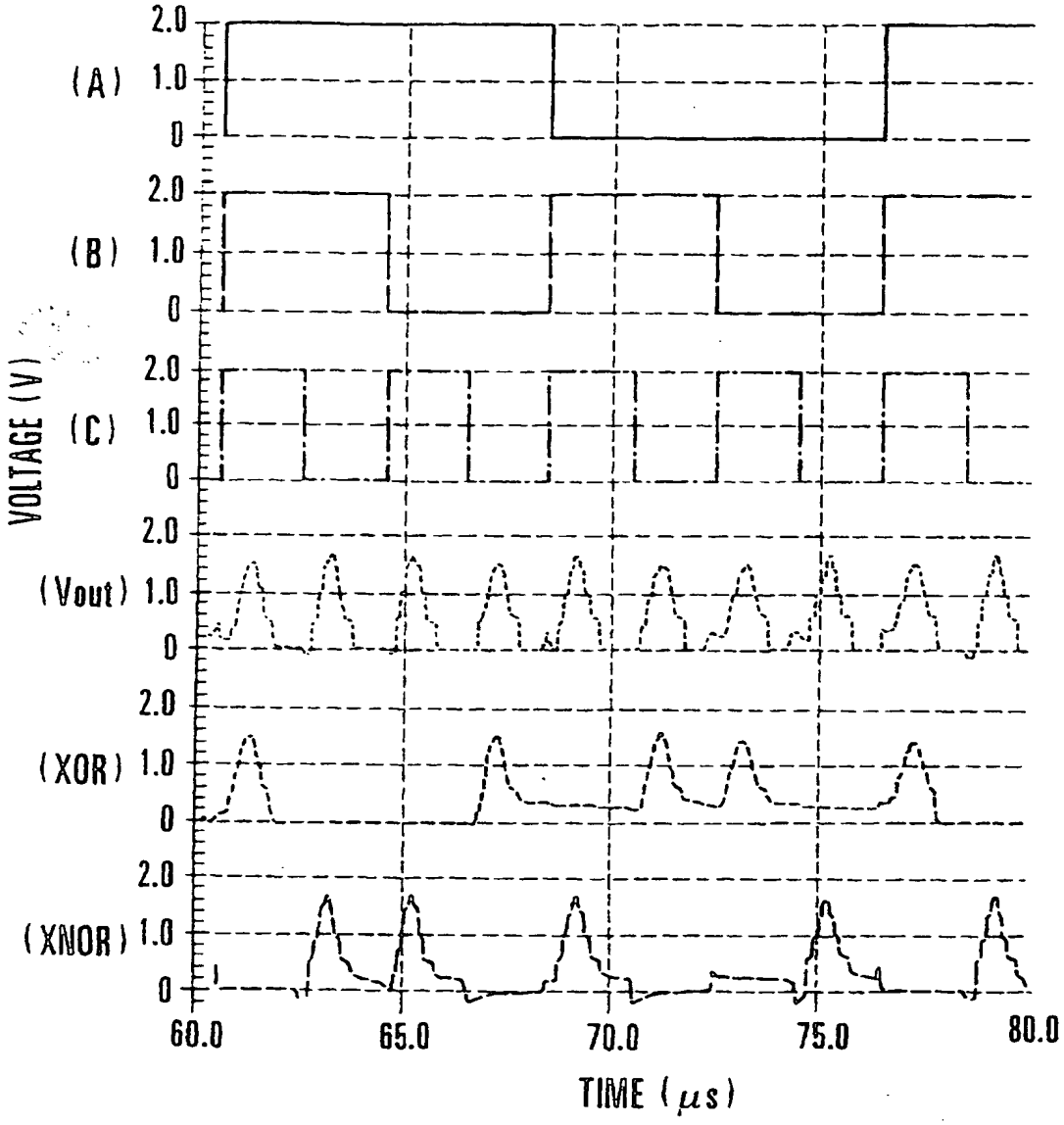


FIG. 12

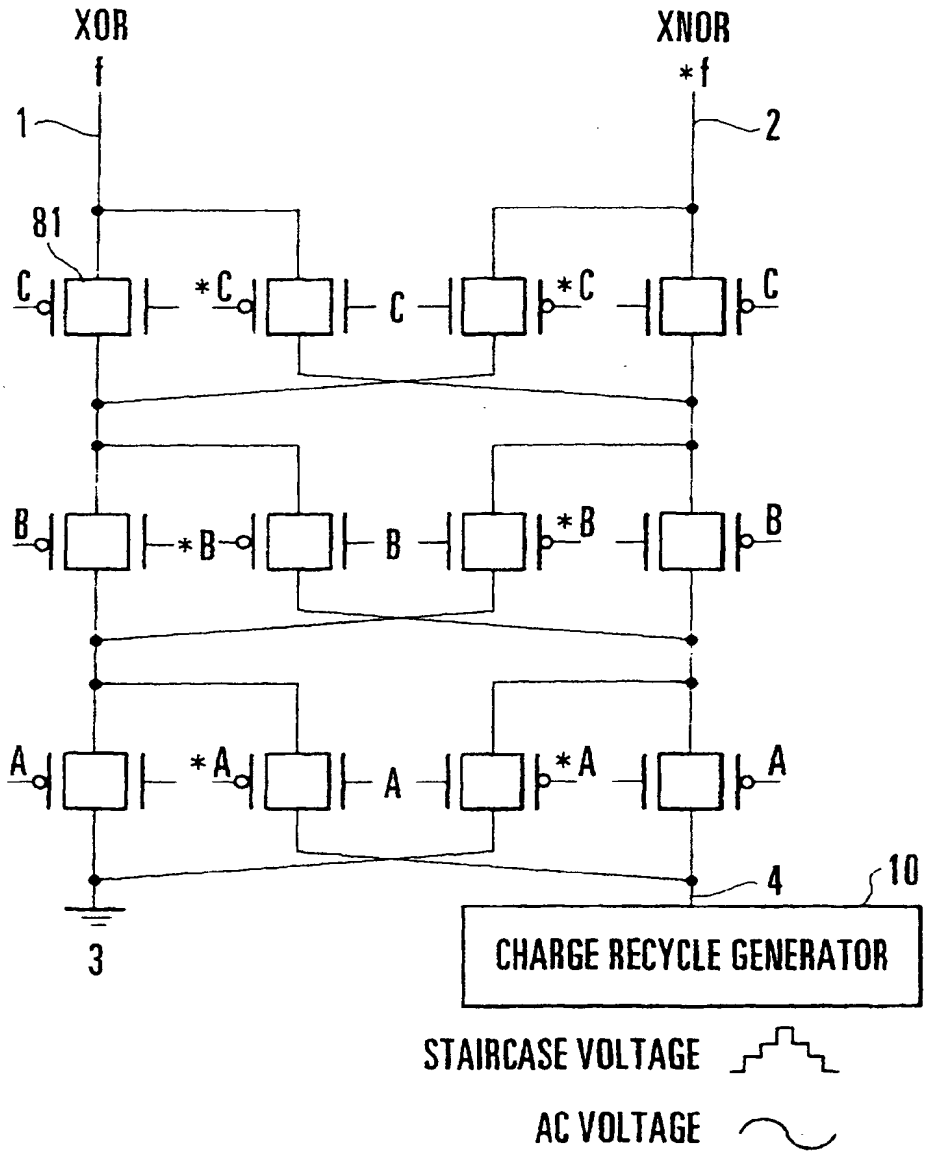


FIG. 13

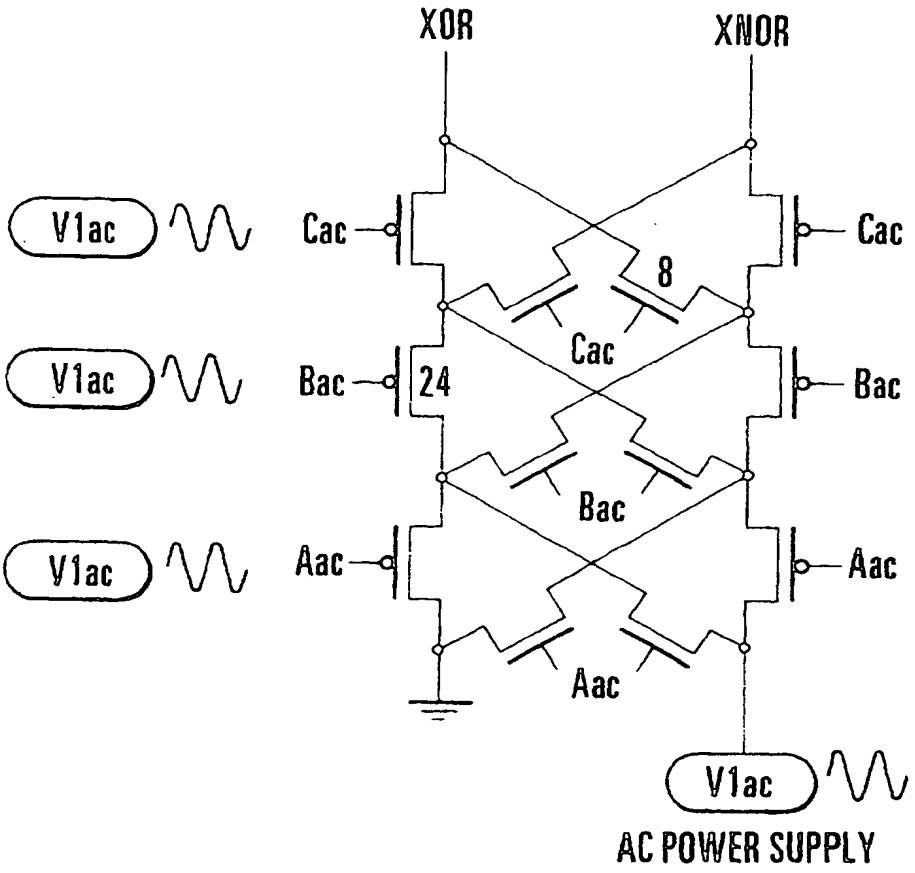


FIG. 14

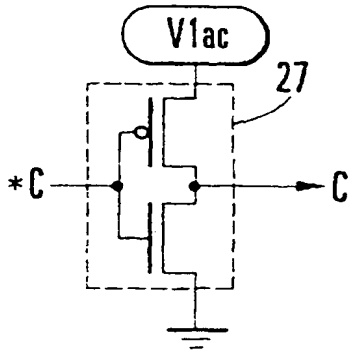


FIG. 15A

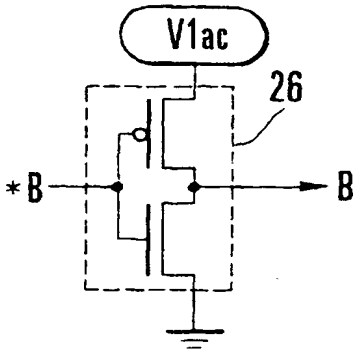


FIG. 15B

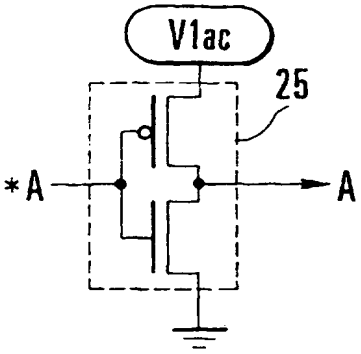


FIG. 15C

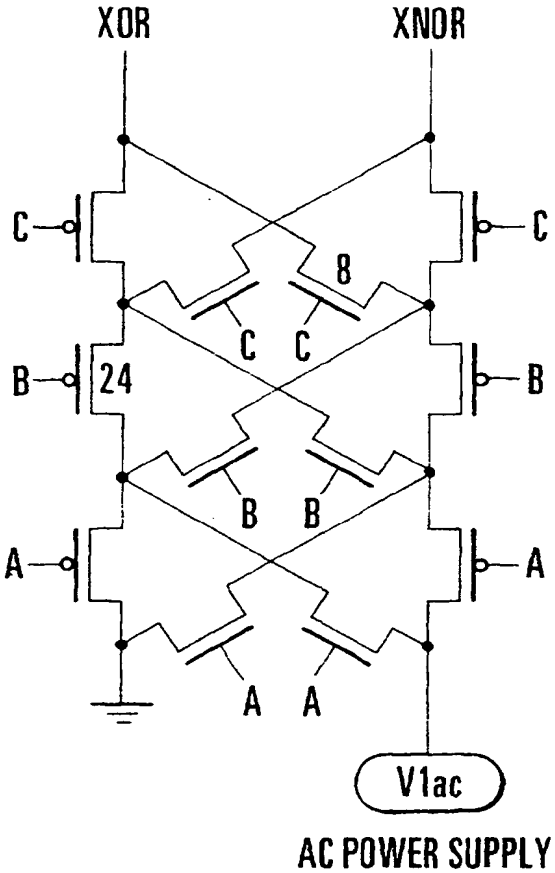


FIG. 15D

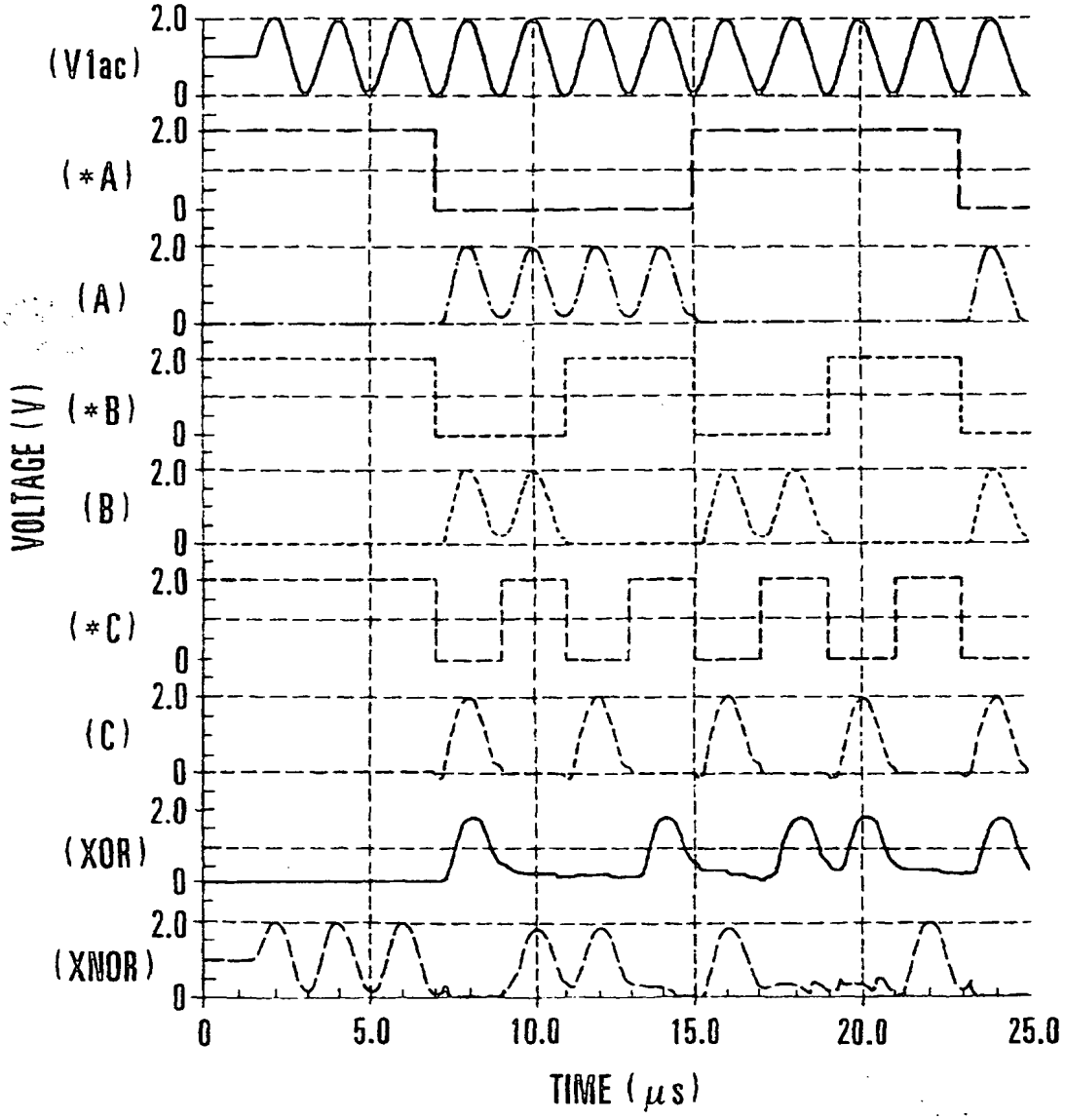


FIG. 16

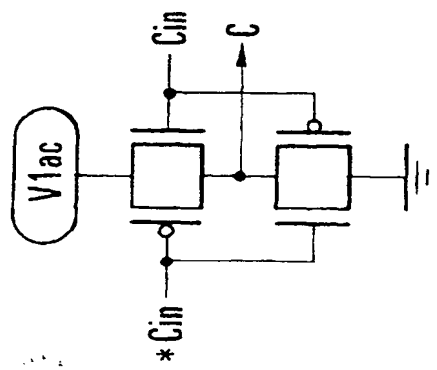


FIG. 17E

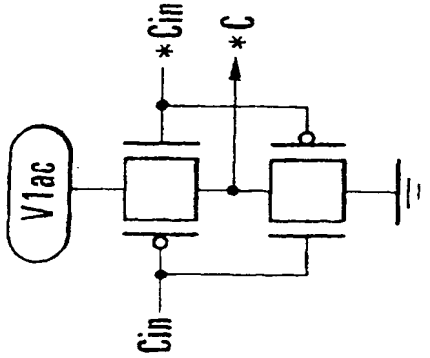


FIG. 17F

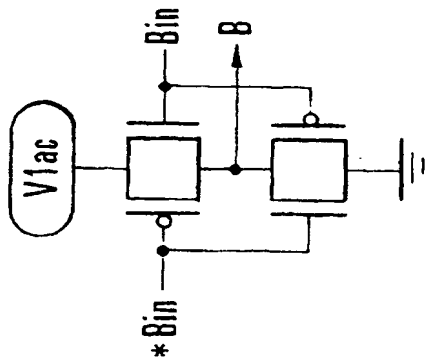


FIG. 17C

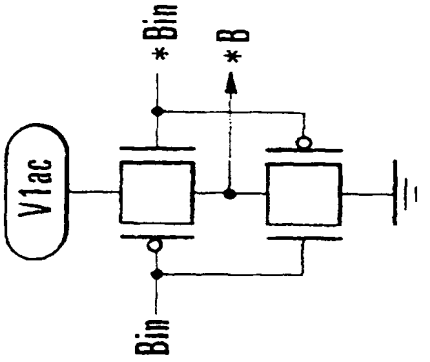


FIG. 17D

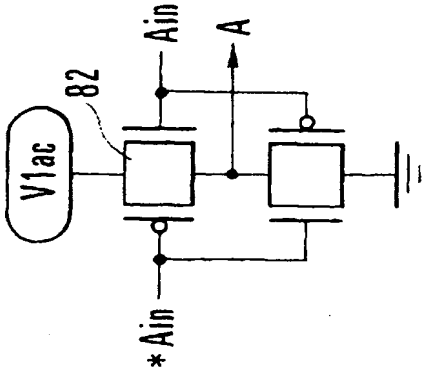


FIG. 17A

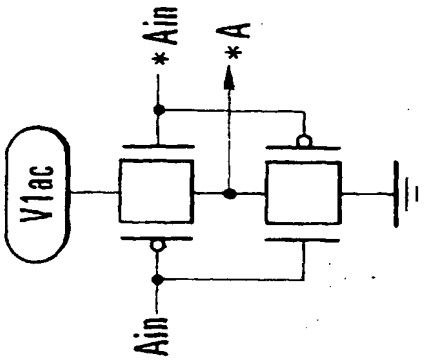


FIG. 17B

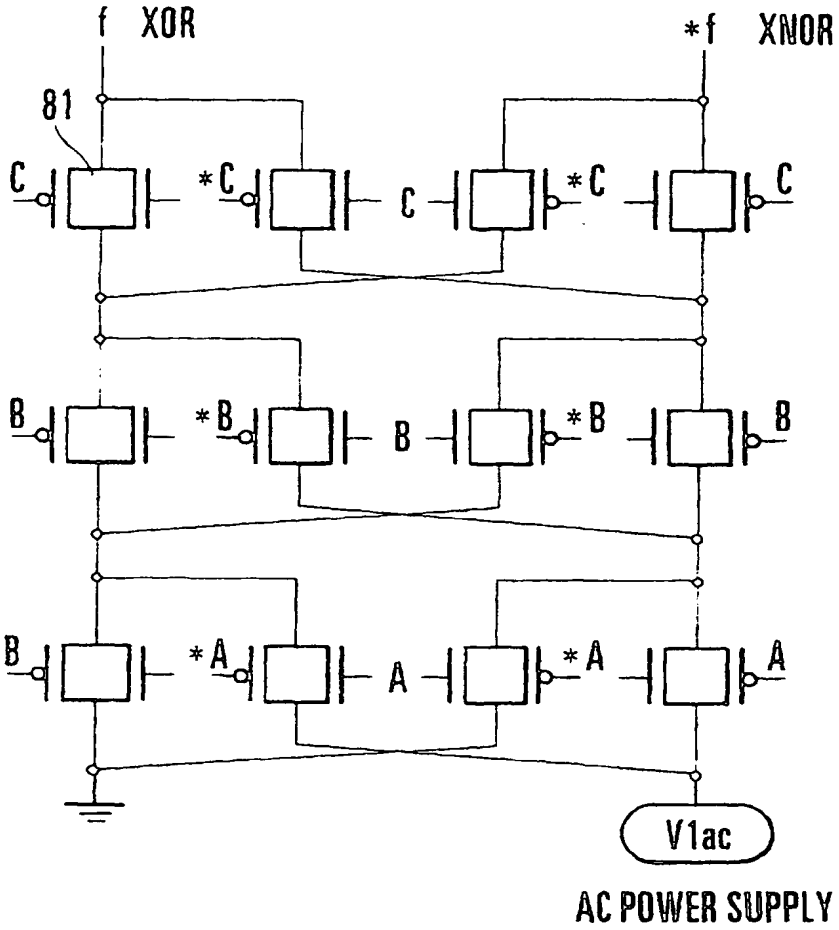


FIG. 17G

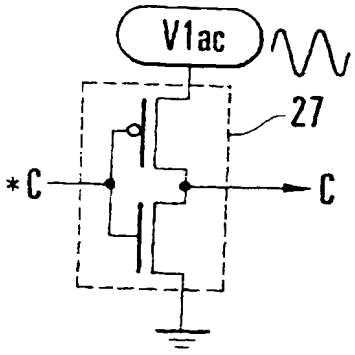


FIG. 18A

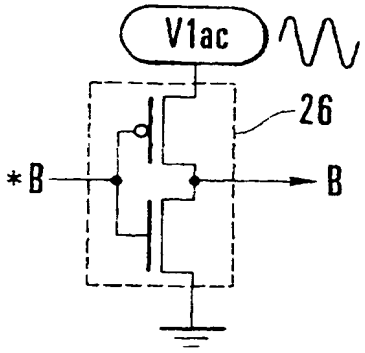


FIG. 18B

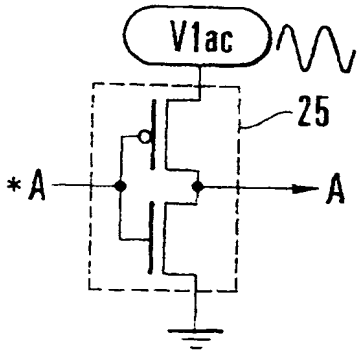


FIG. 18C

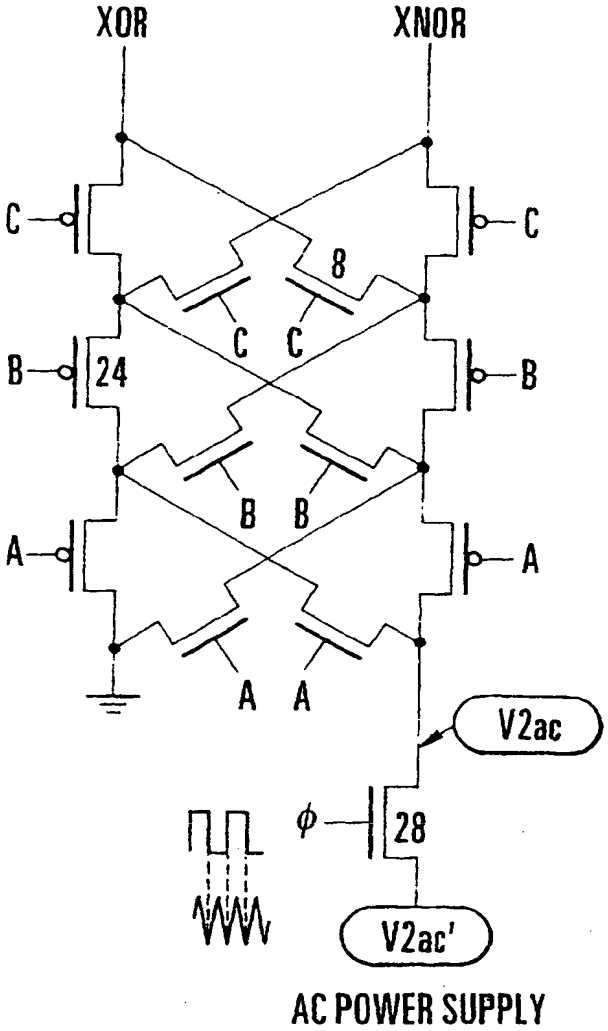


FIG. 18D

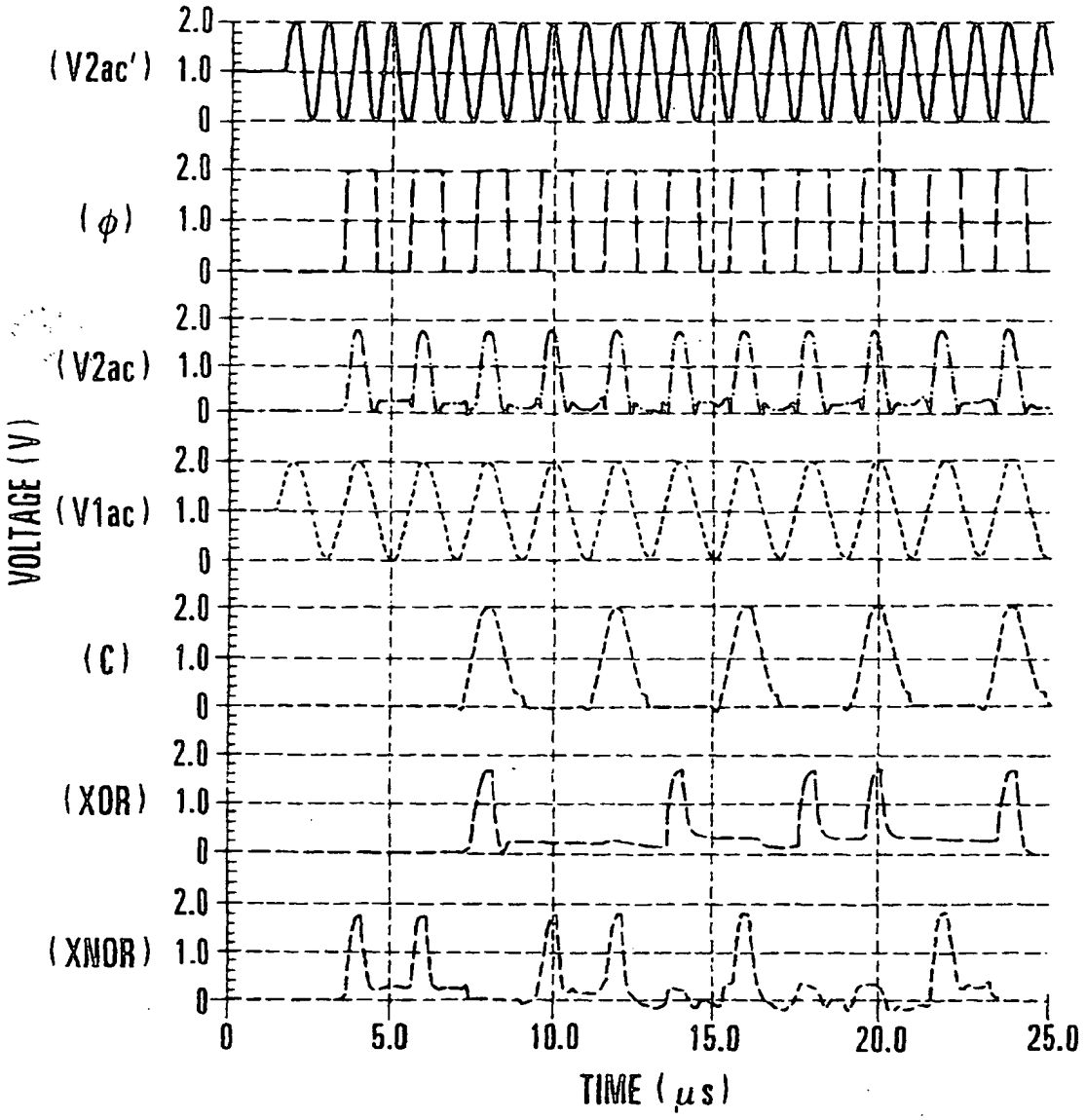


FIG. 19

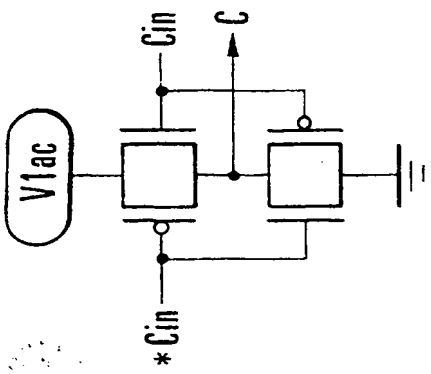


FIG. 20E

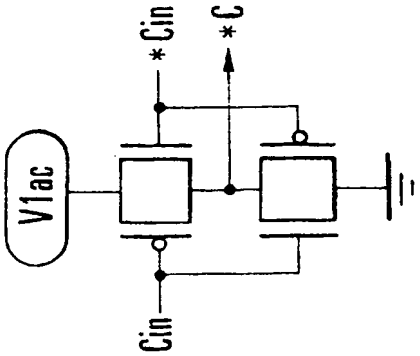


FIG. 20F

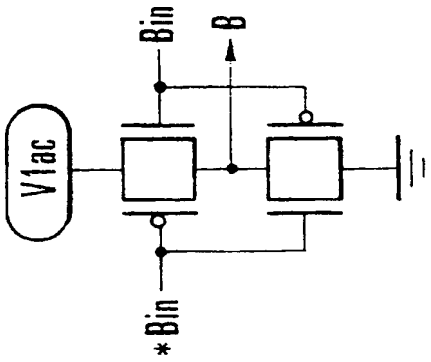


FIG. 20C

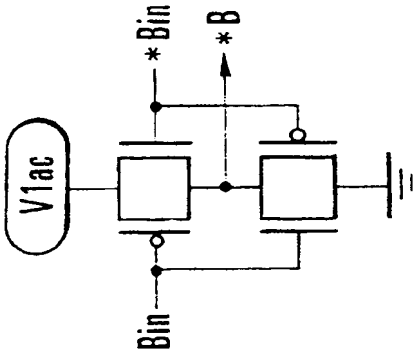


FIG. 20D

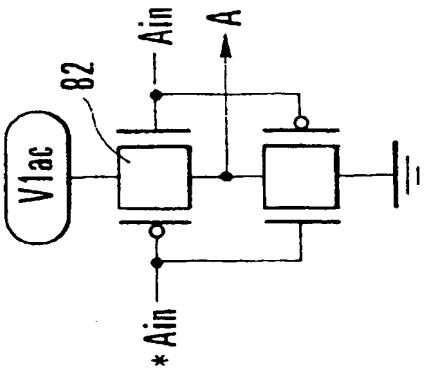


FIG. 20A

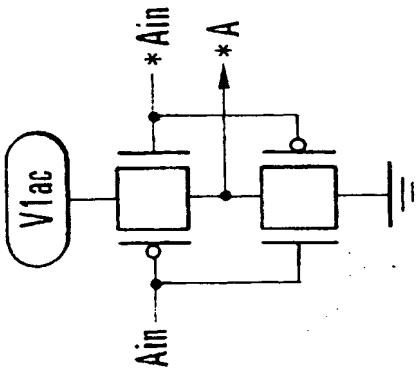


FIG. 20B

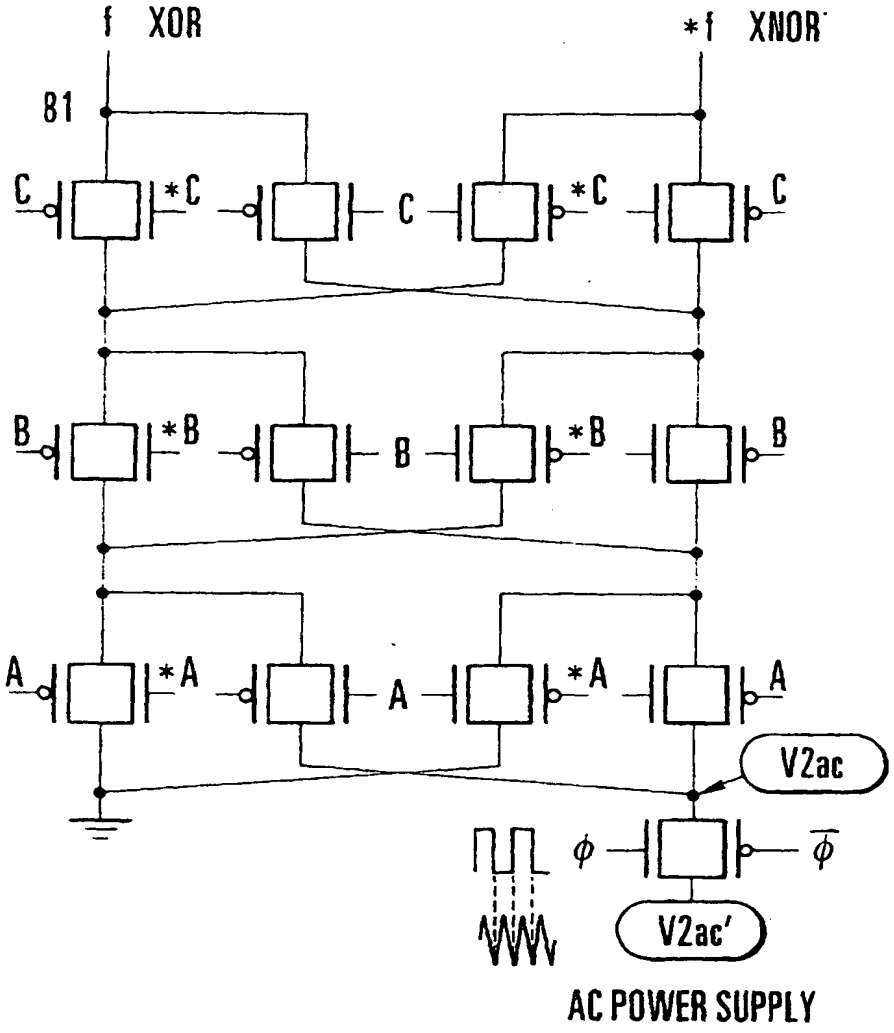


FIG. 20G

FIG.21A

BOTH V1ac AND V2ac ARE TRAPEZOIDAL WAVEFORMS

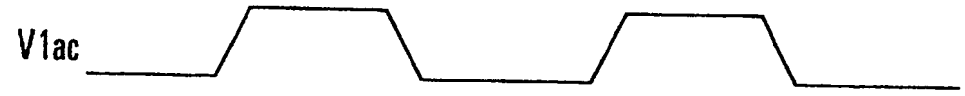


FIG.21B

FIG.21C

V1ac IS TRAPEZOIDAL WAVEFORM ; V2ac IS TRIANGULAR WAVEFORM

FIG.21D

FIG.21E

BOTH V1ac AND V2ac ARE AC VOLTAGES BASED ON SINE WAVE

FIG.21F

FIG.21G

BOTH V1ac AND V2ac ARE STAIRCASE WAVEFORMS FORMED BY POWER SUPPLY CIRCUIT 10B

FIG.21H

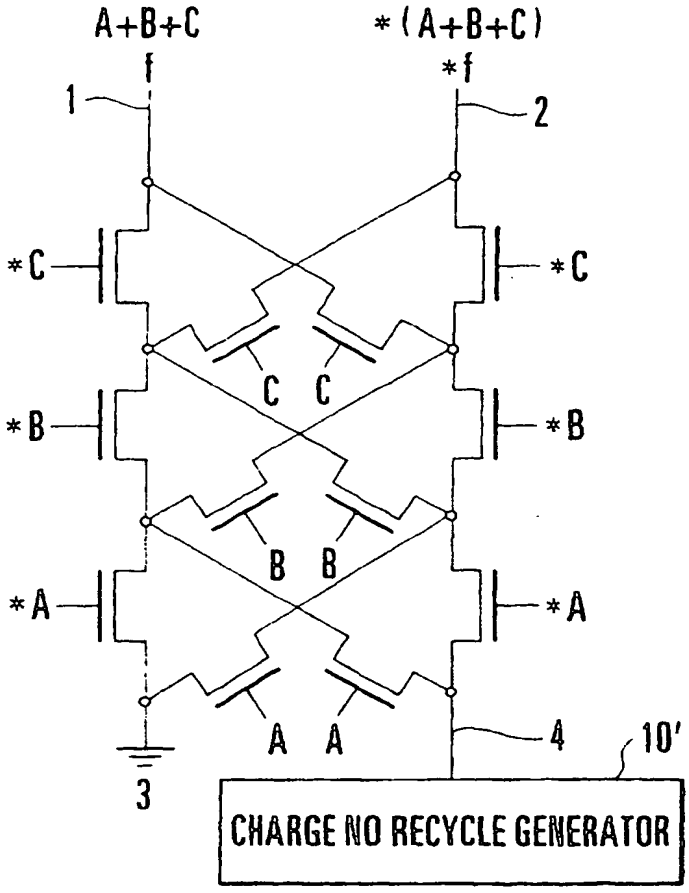


FIG. 22A

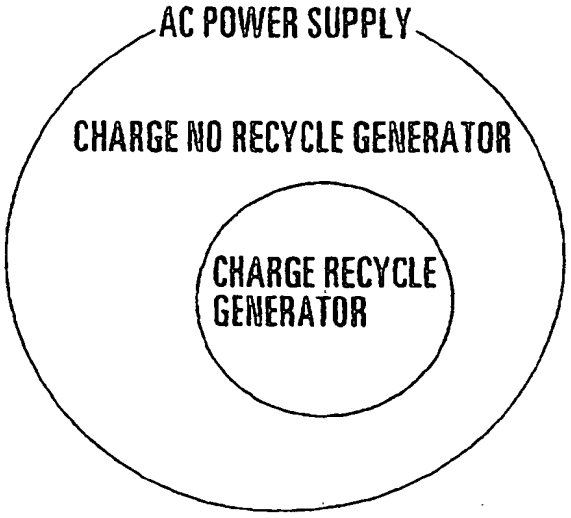


FIG. 22B

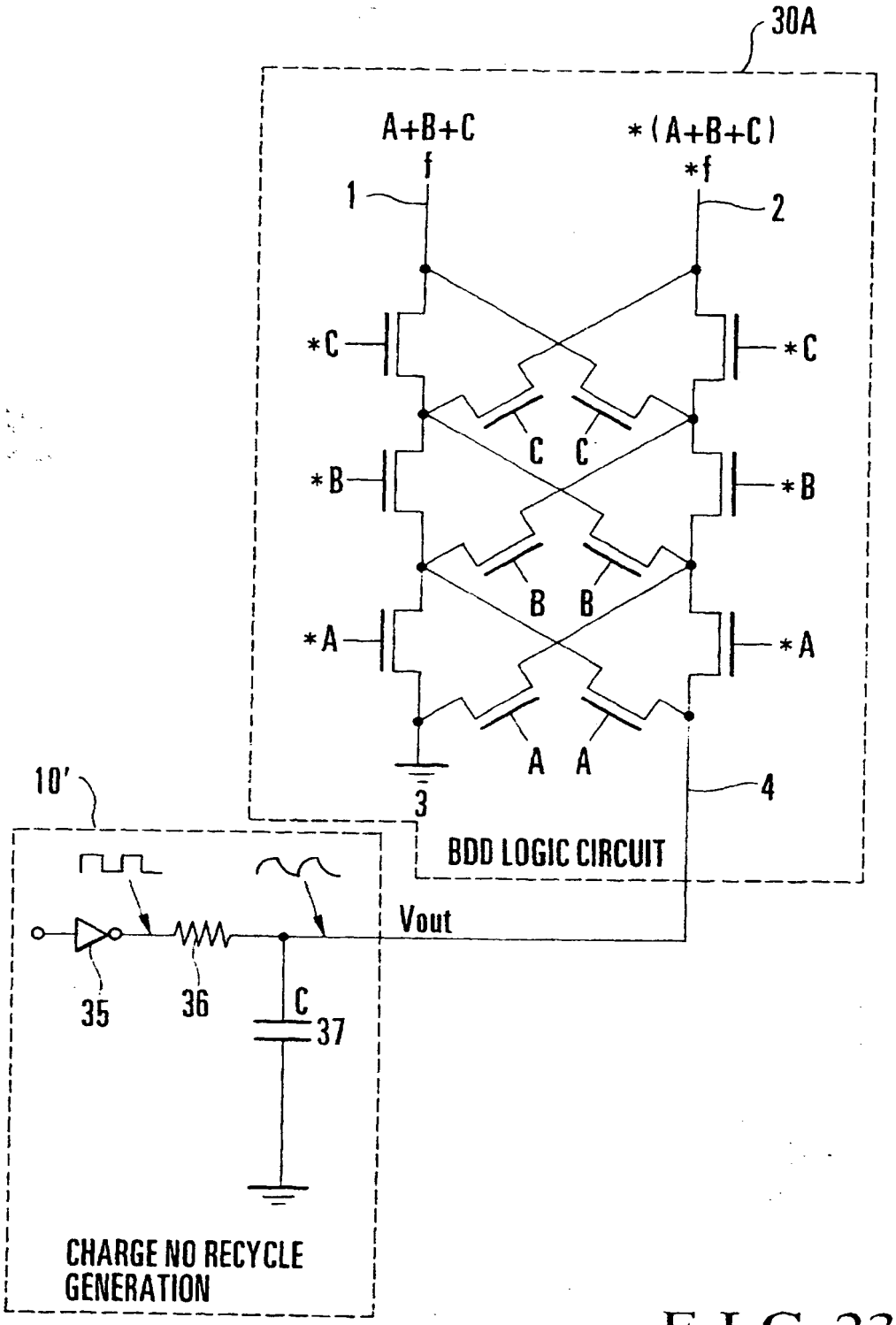


FIG. 23

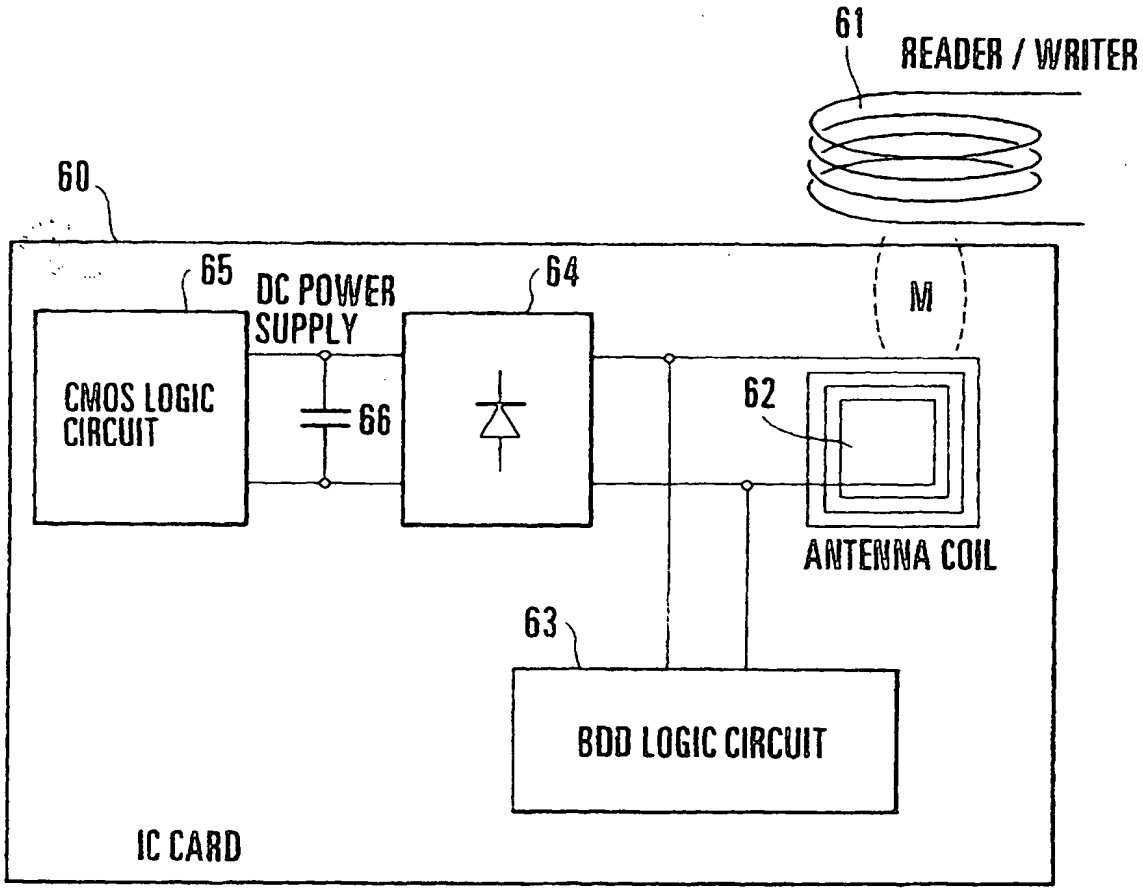


FIG. 24

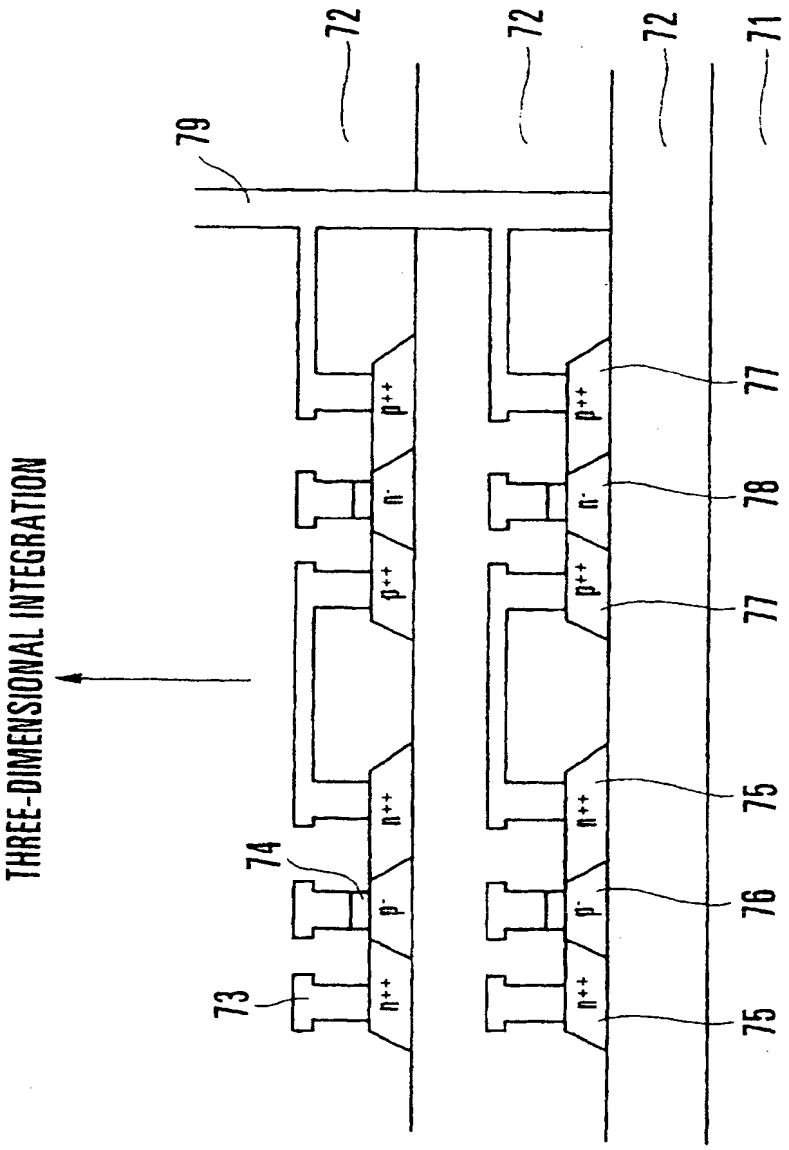


FIG. 25

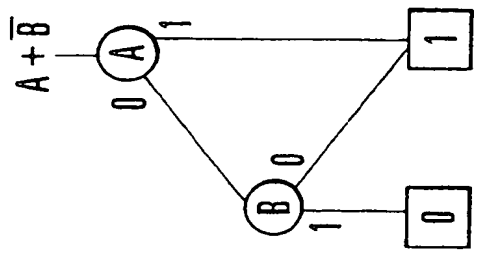


FIG. 26D

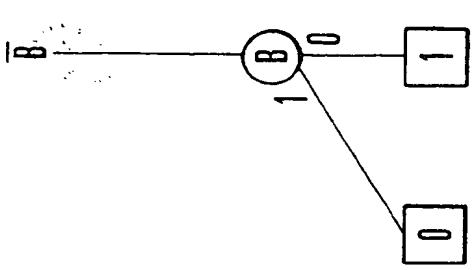


FIG. 26C

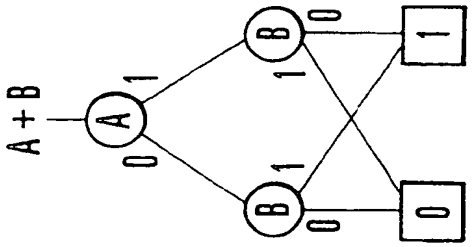


FIG. 26B

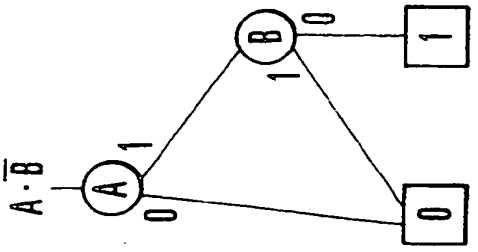


FIG. 26A

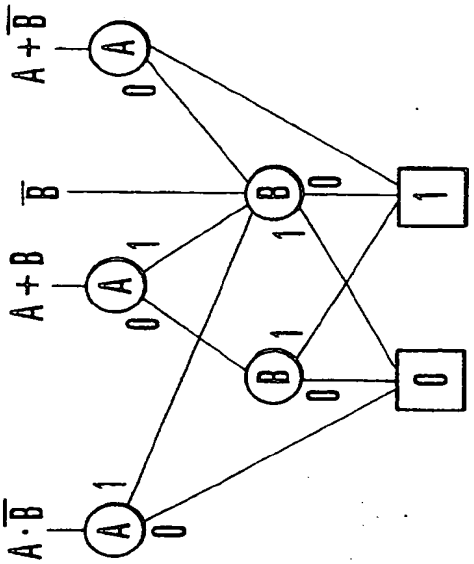


FIG. 26E

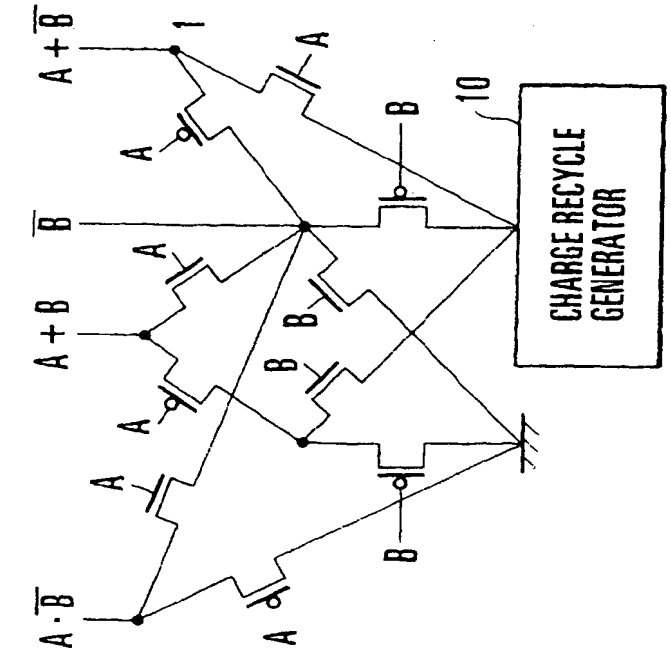


FIG. 27B

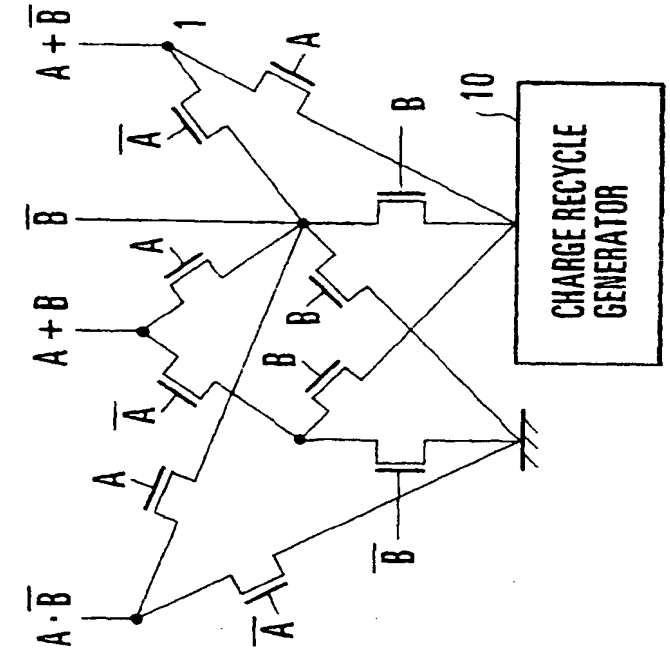


FIG. 27A

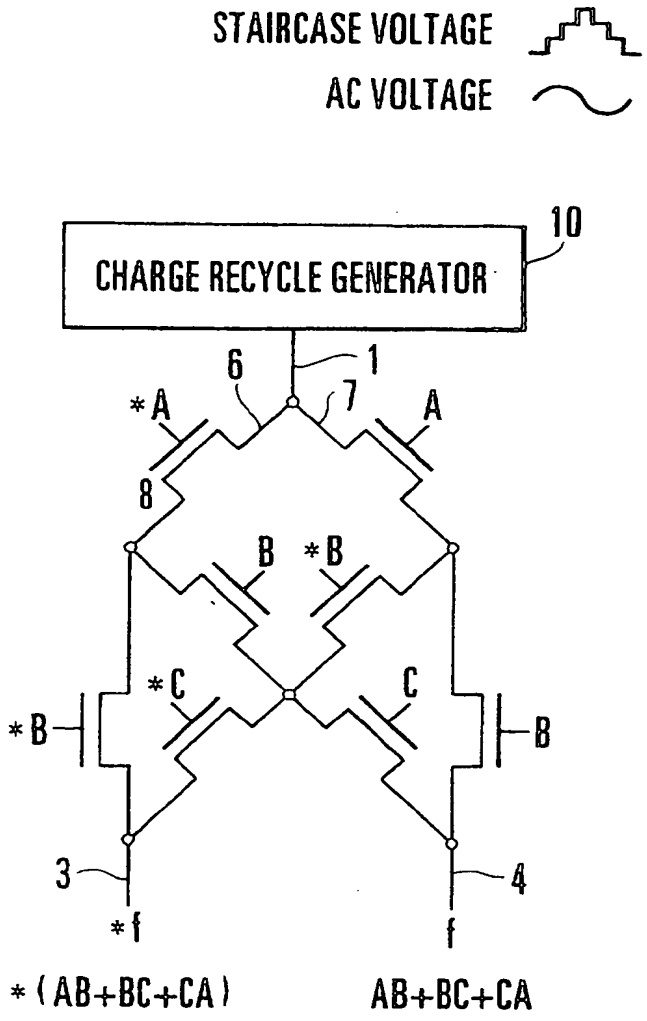


FIG. 28

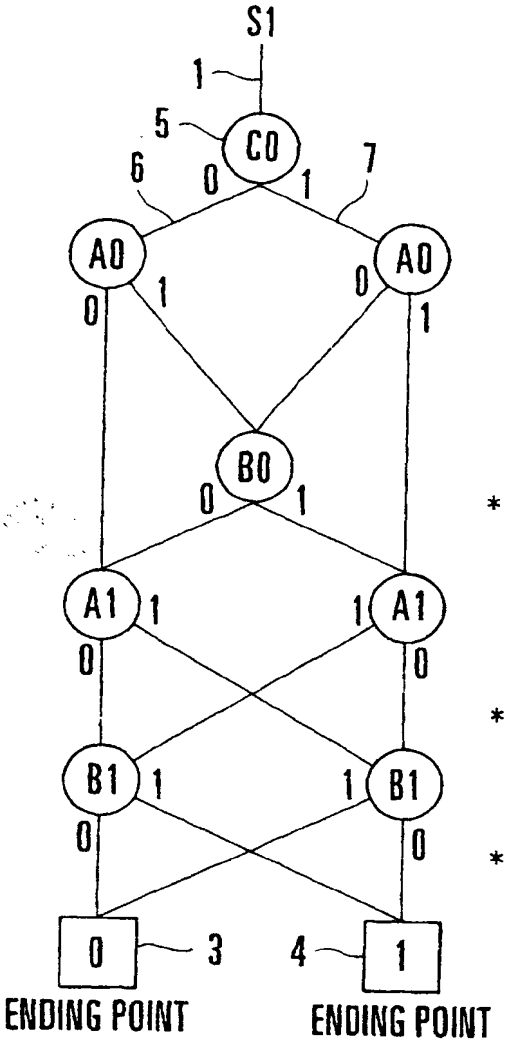


FIG. 29A

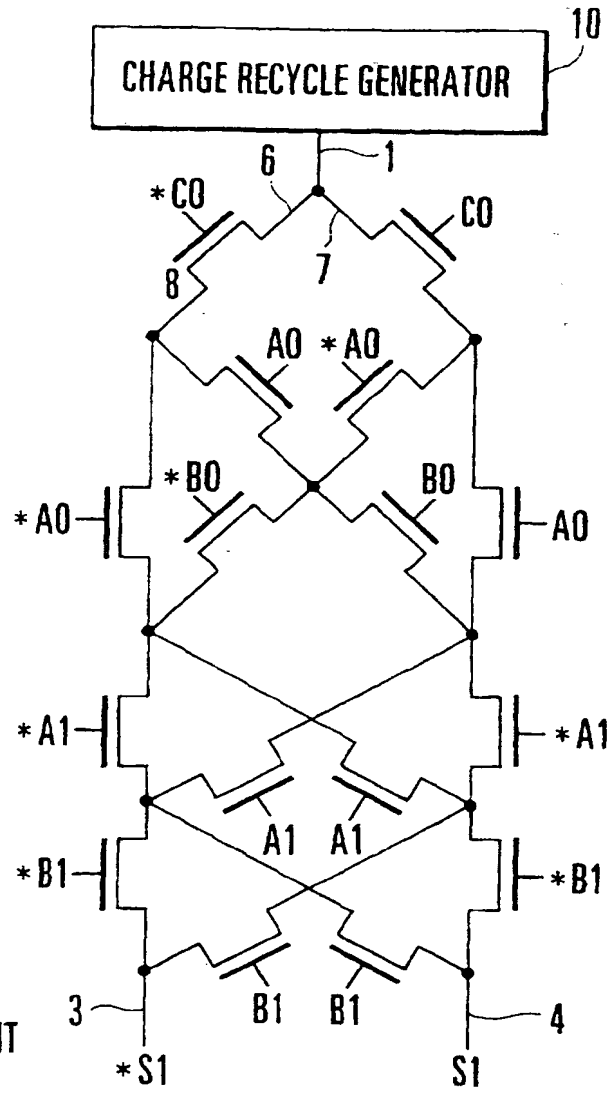


FIG. 29B

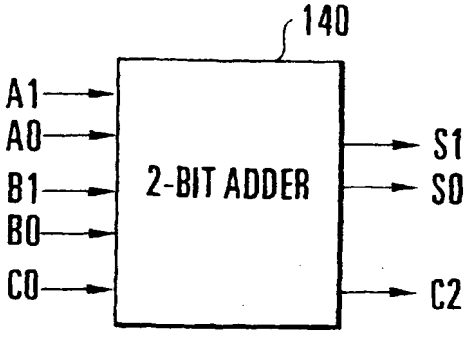


FIG. 29C

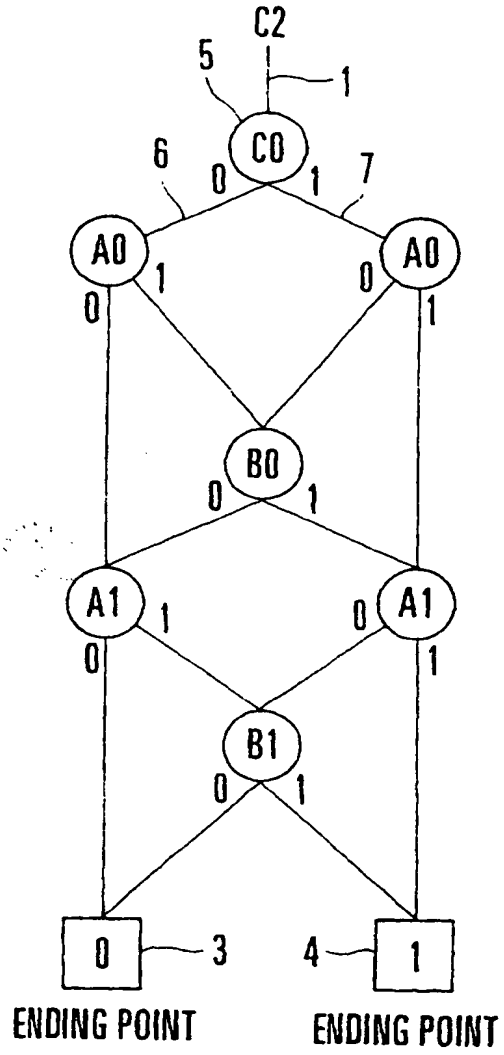


FIG. 30A

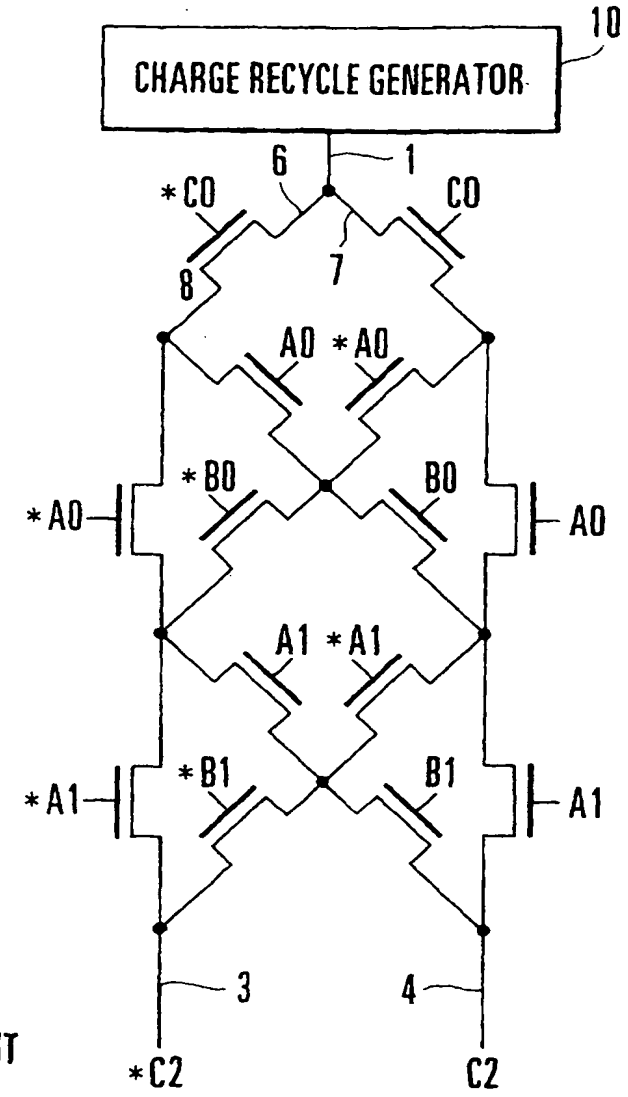


FIG. 30B

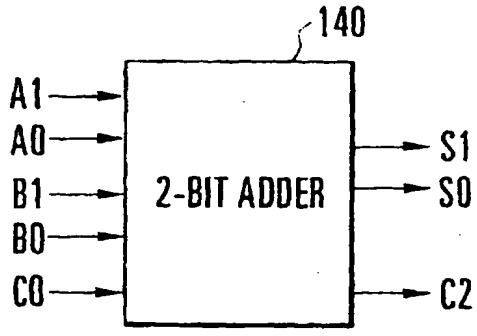


FIG. 30C

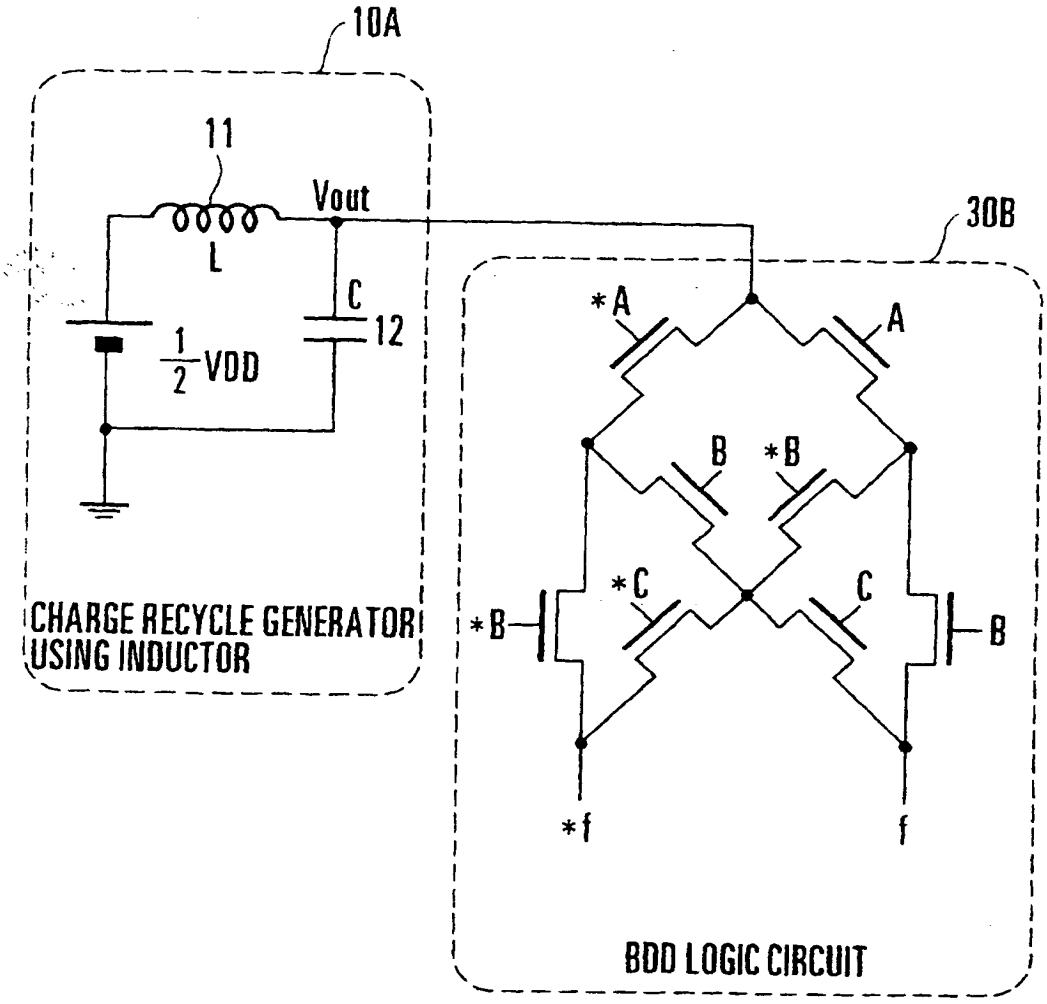


FIG. 31

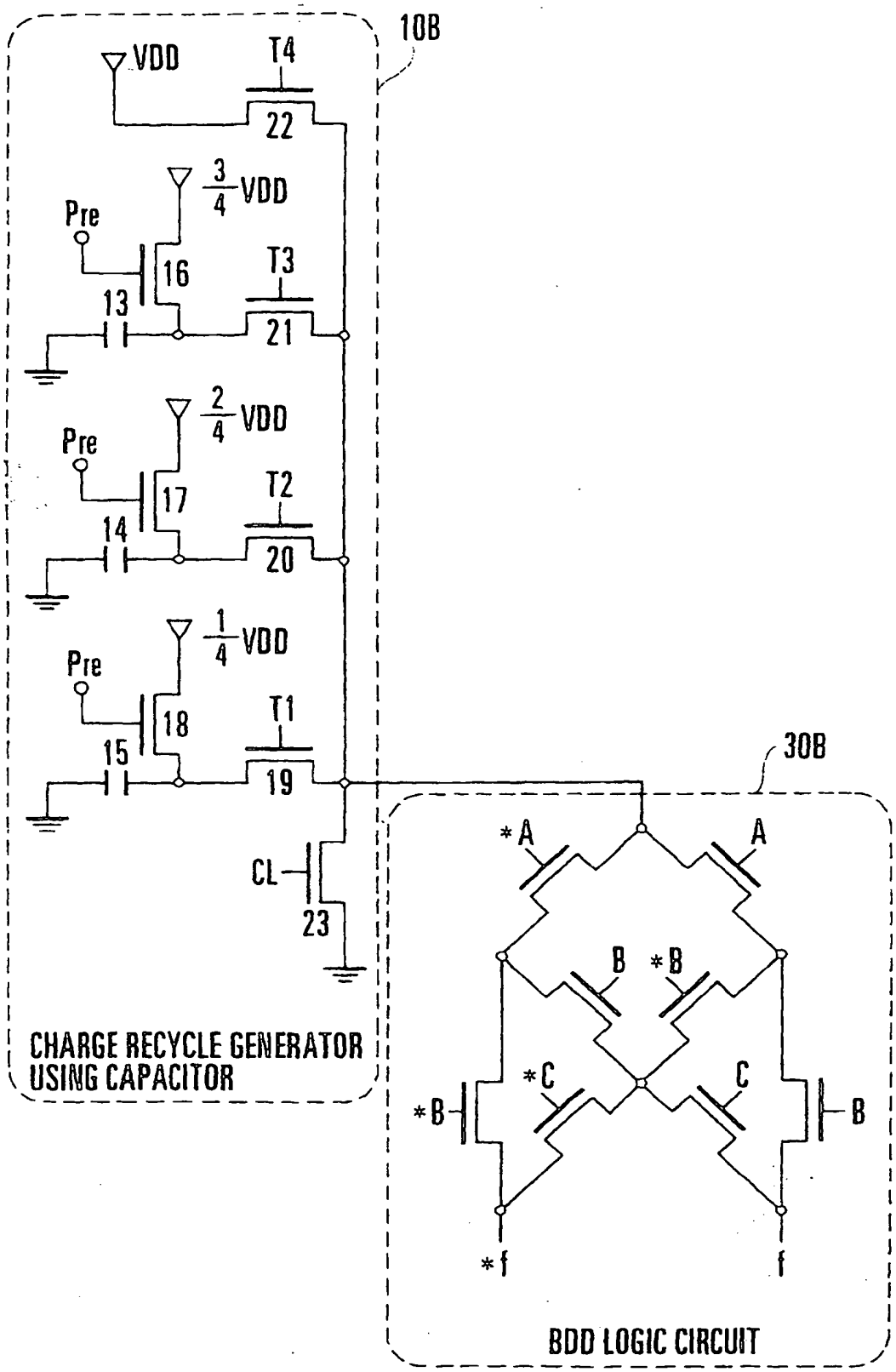


FIG. 32

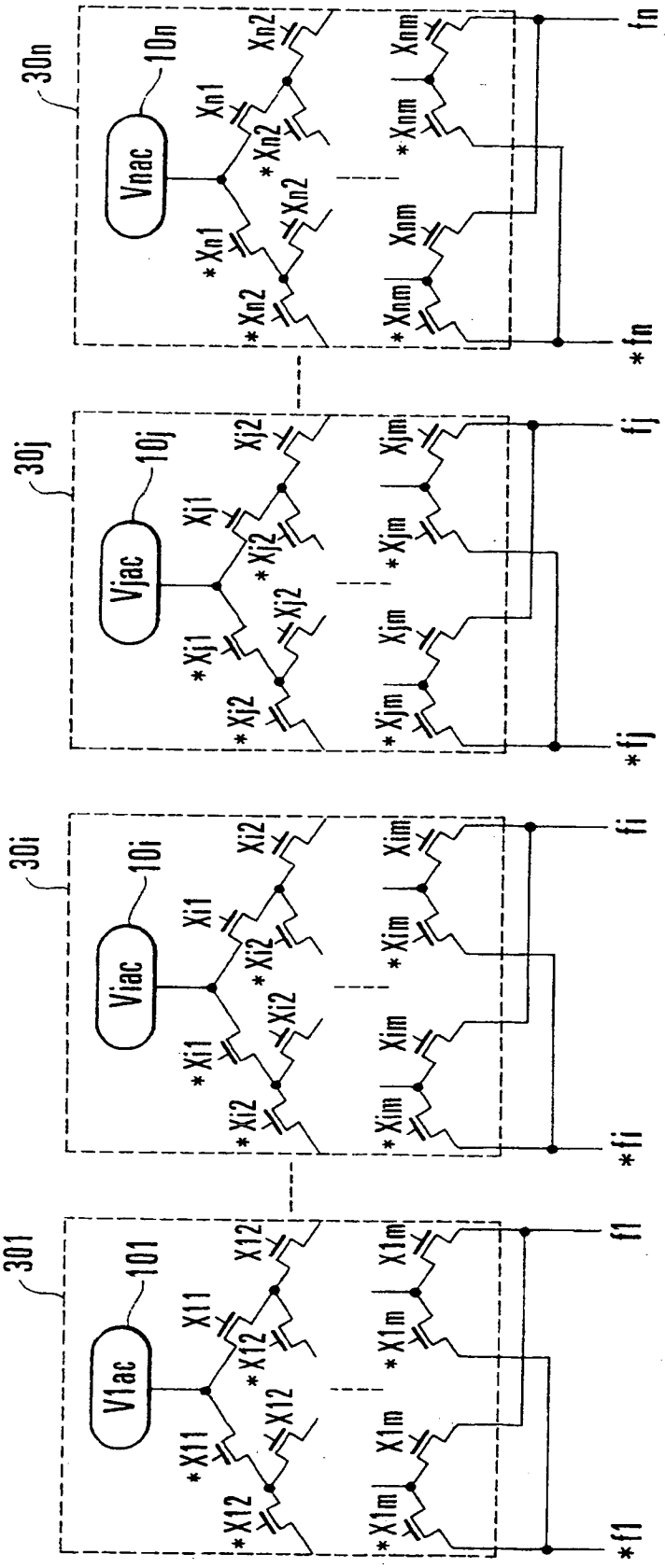


FIG. 33

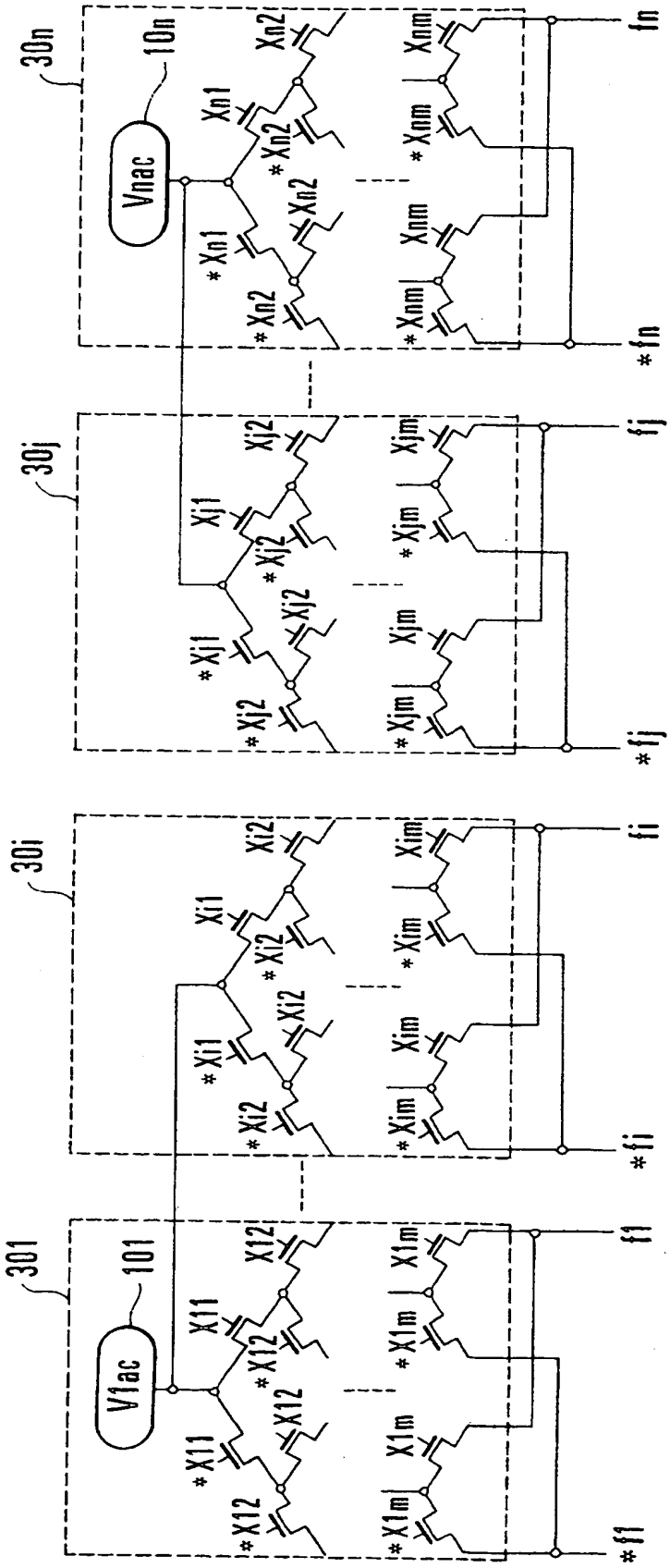


FIG. 34

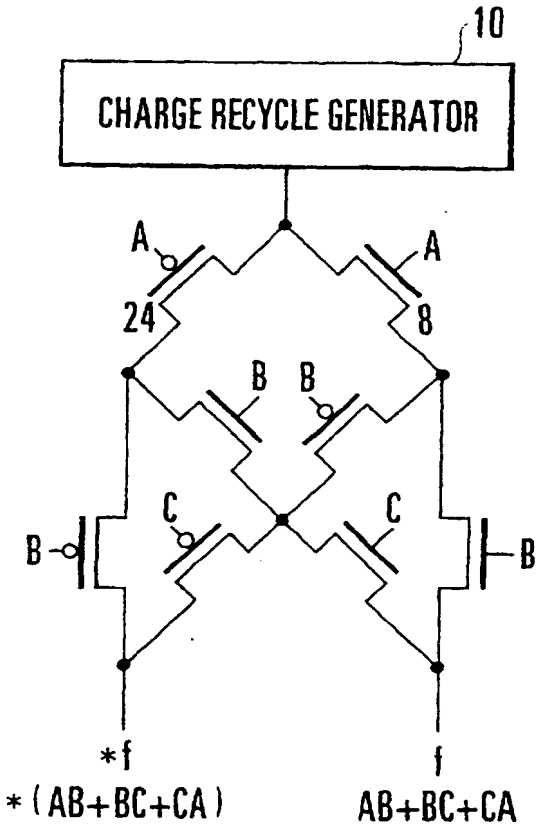


FIG. 35

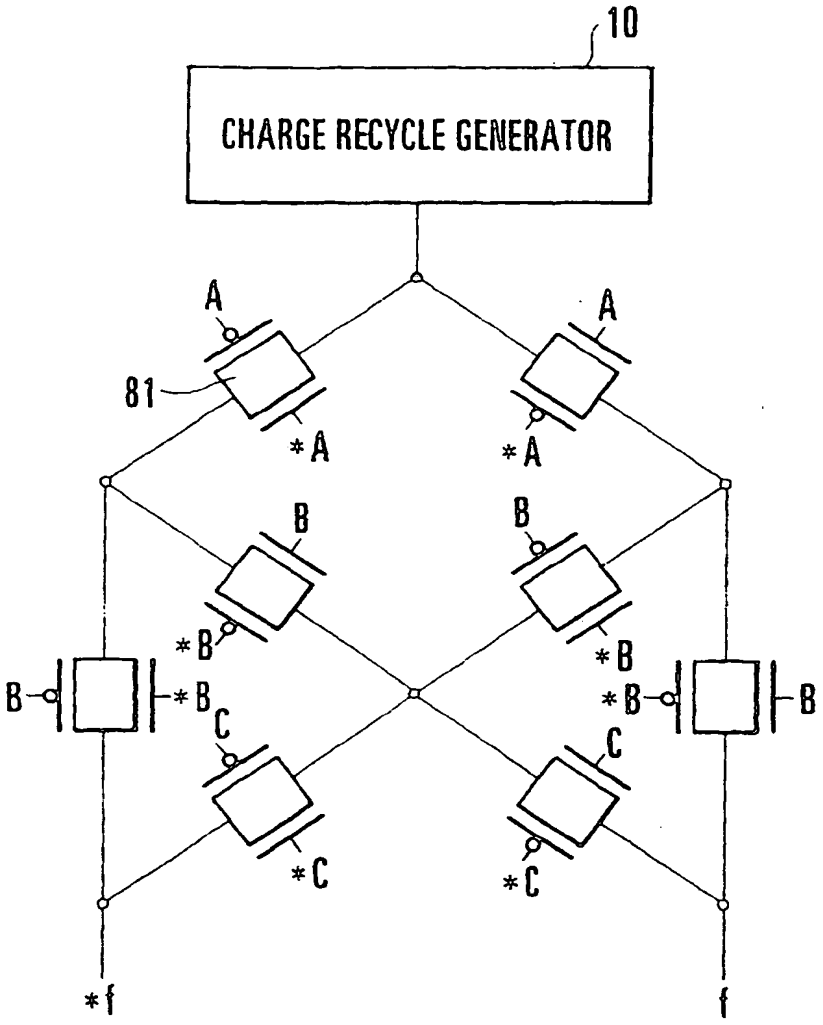


FIG. 36

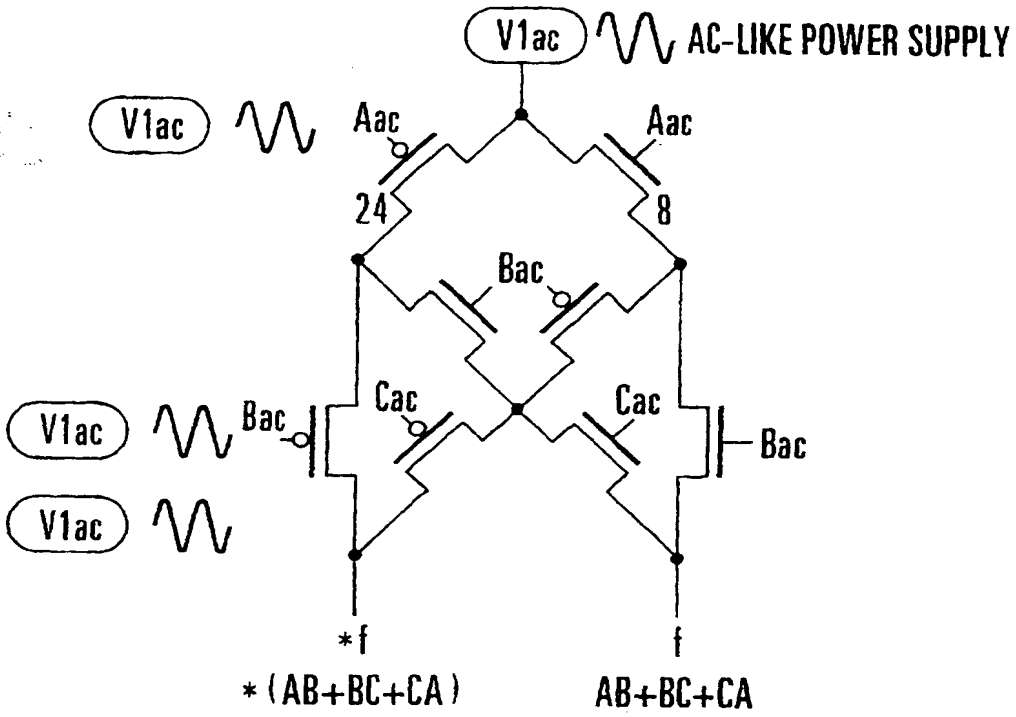


FIG. 37

FIG.38A

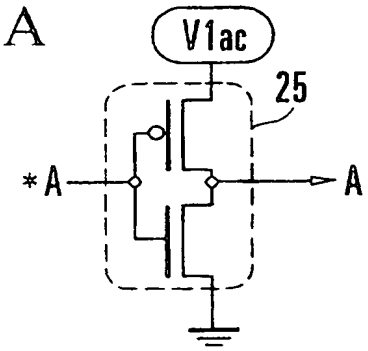


FIG.38B

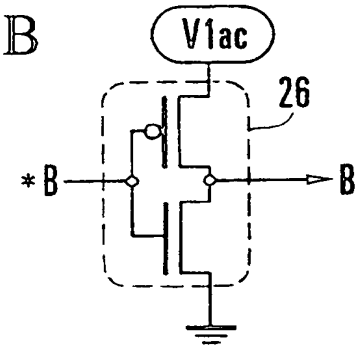
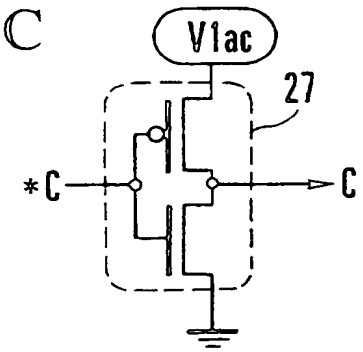


FIG.38C



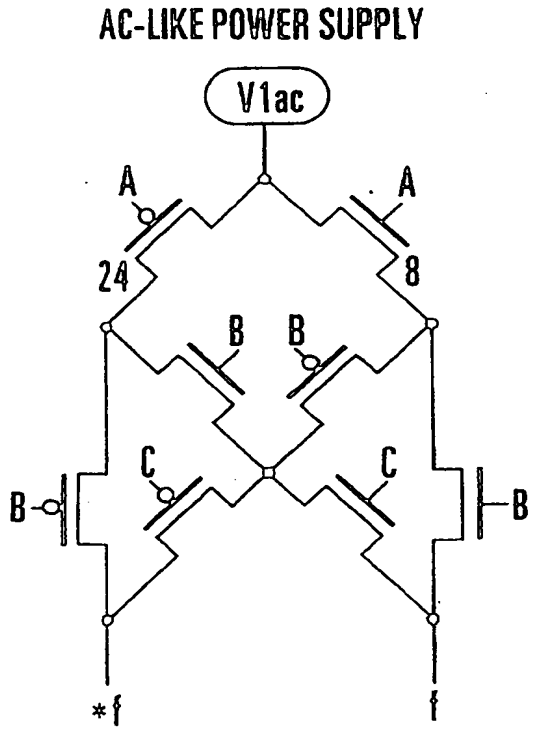


FIG.38D

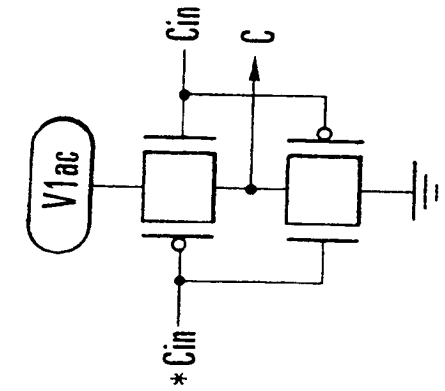


FIG. 39E

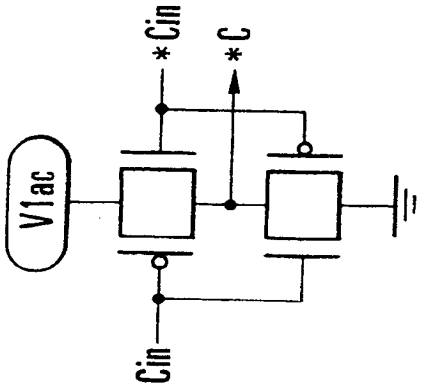


FIG. 39F

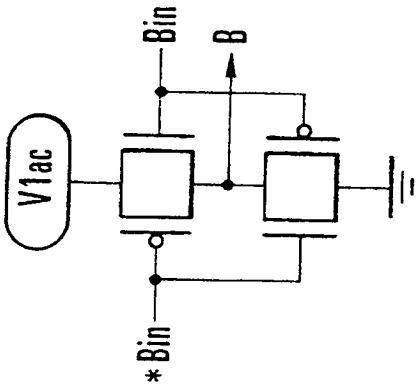


FIG. 39C

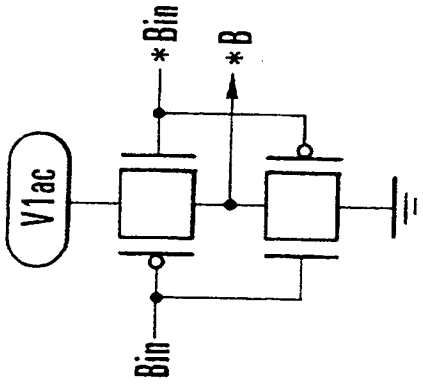


FIG. 39D

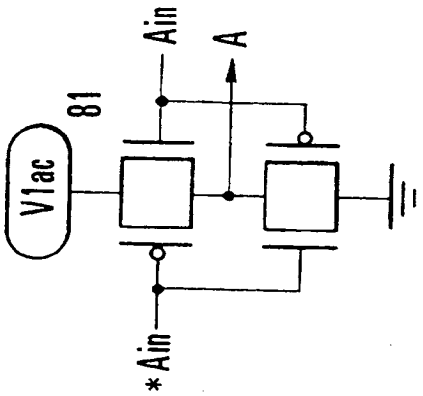


FIG. 39A

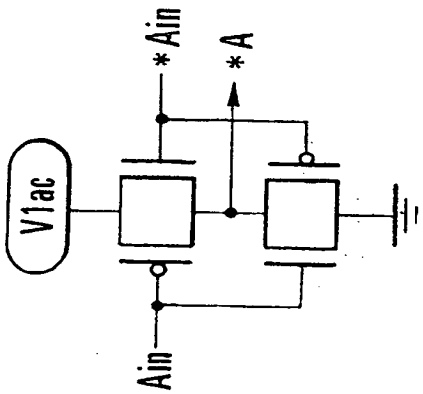


FIG. 39B

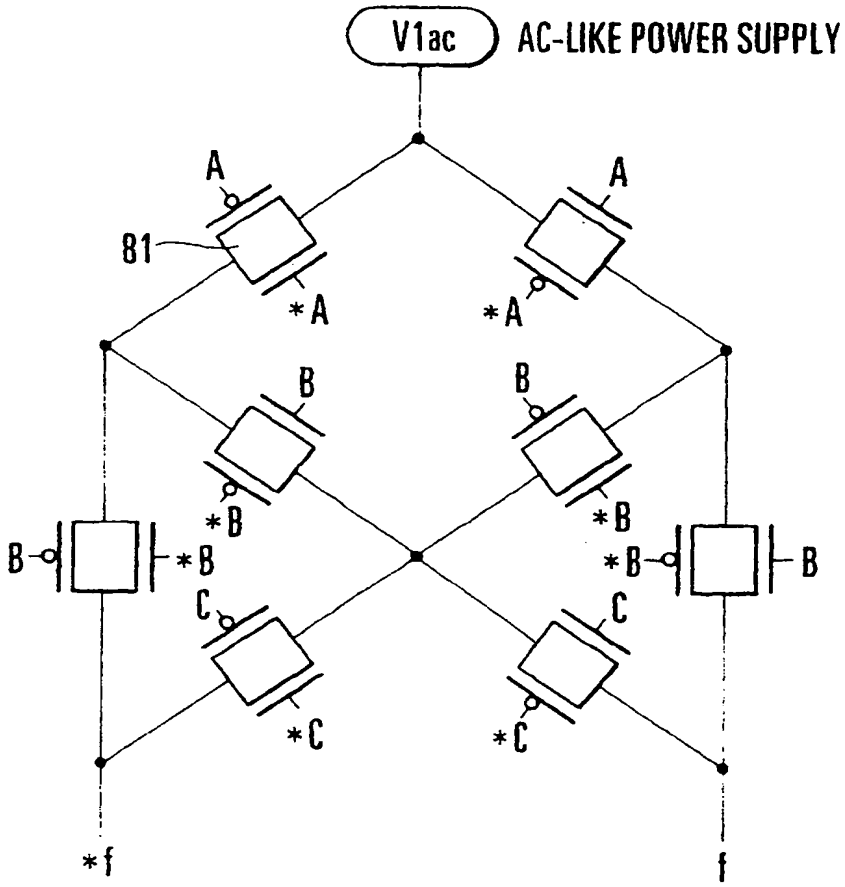


FIG. 39G

FIG.40A

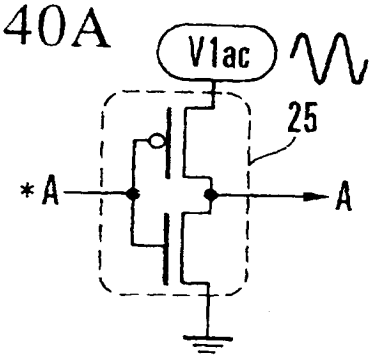


FIG.40B

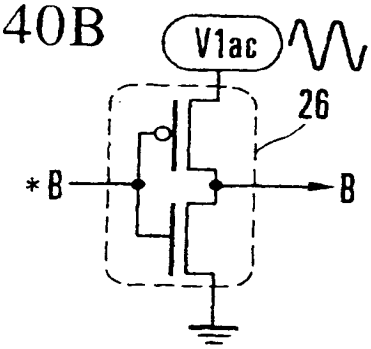
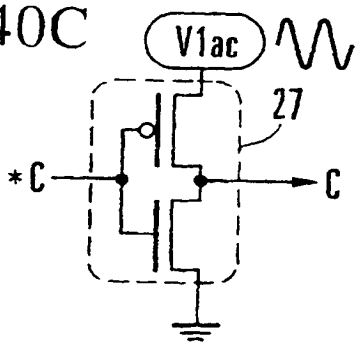


FIG.40C



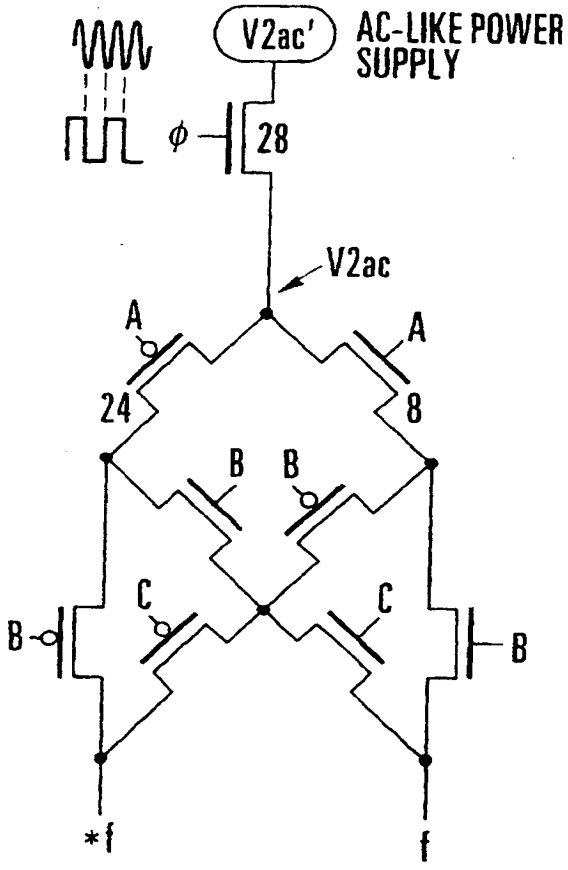


FIG.40D

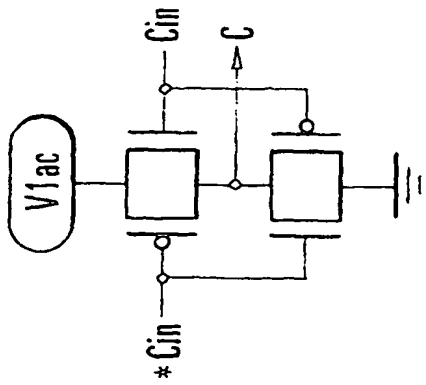


FIG. 41E

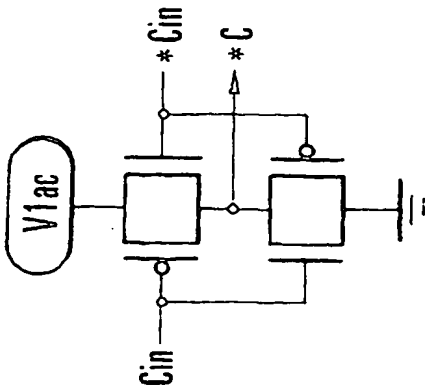


FIG. 41F

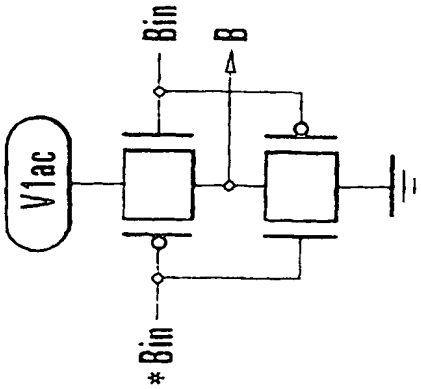


FIG. 41C

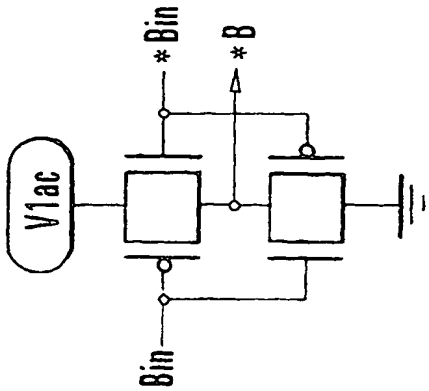


FIG. 41D

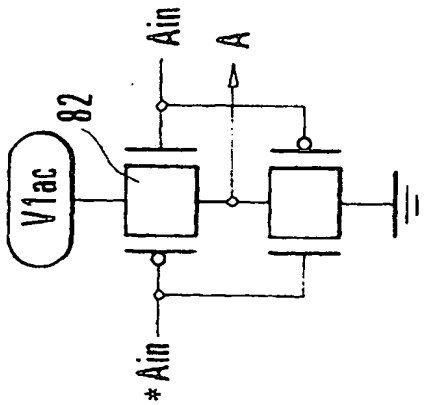


FIG. 41A

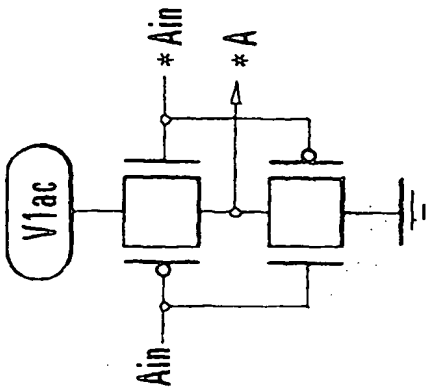


FIG. 41B

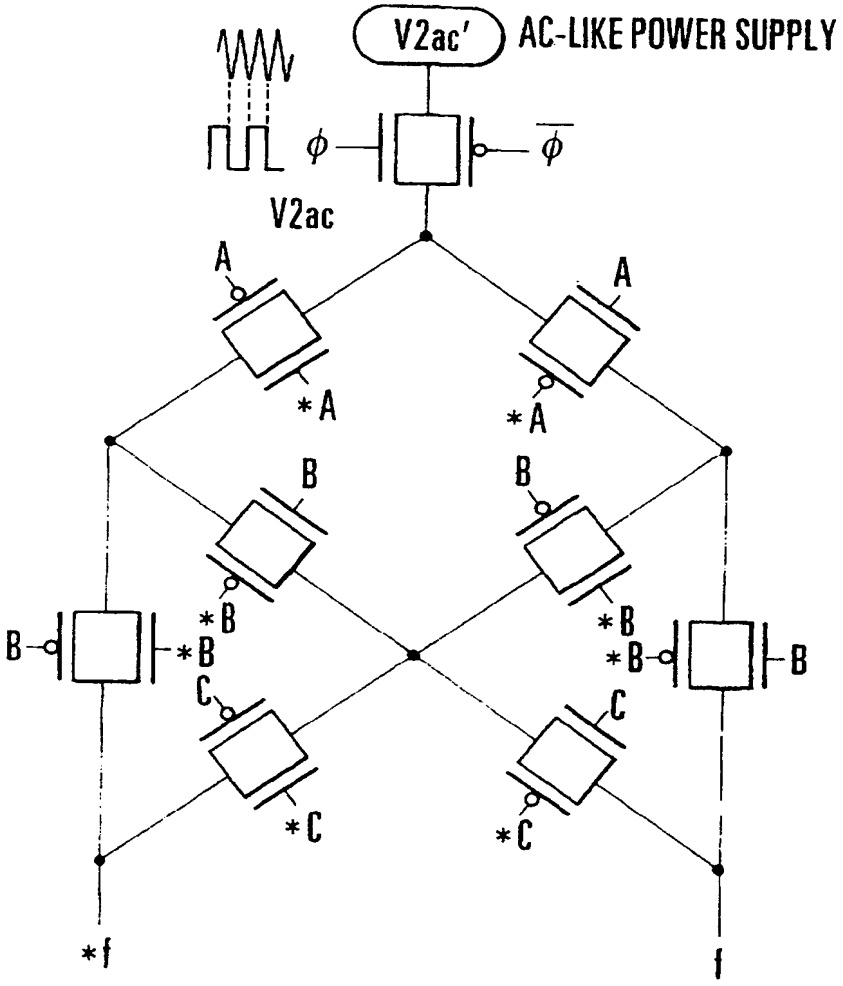


FIG. 41G

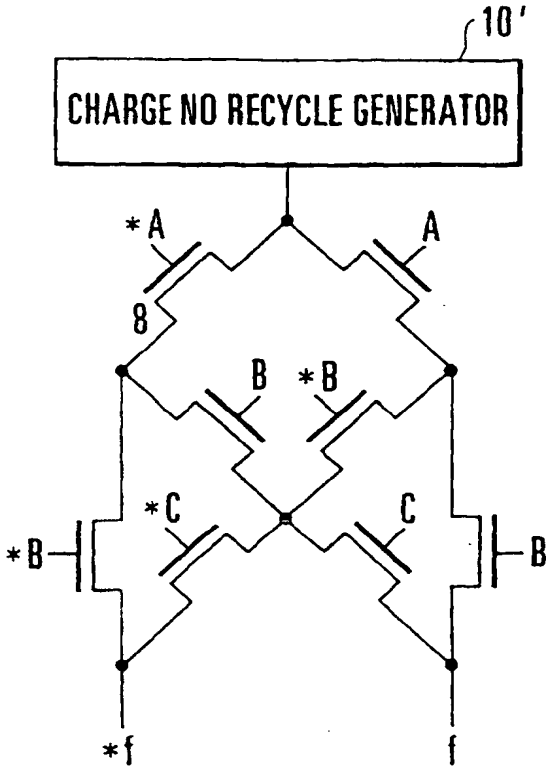


FIG. 42A

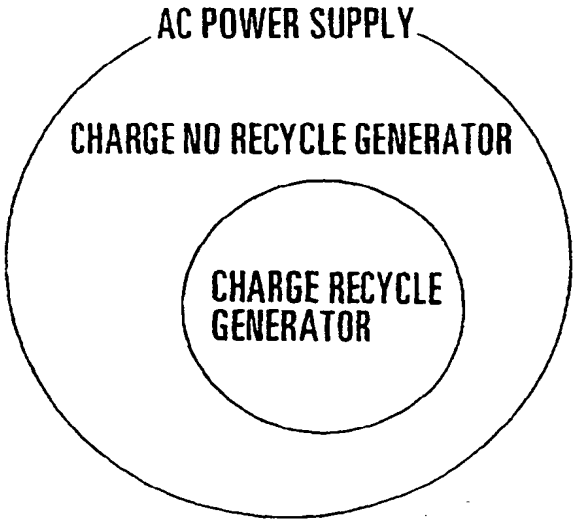


FIG. 42B

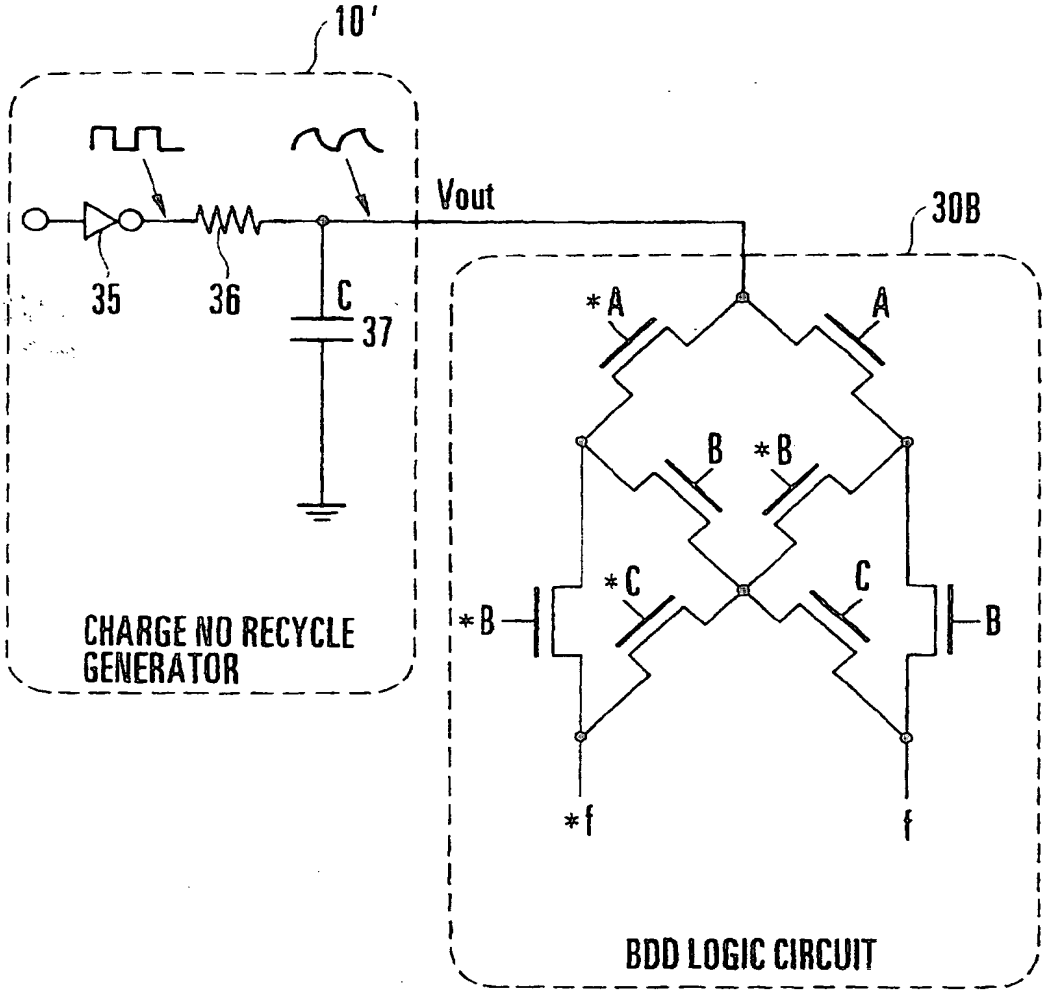


FIG. 43

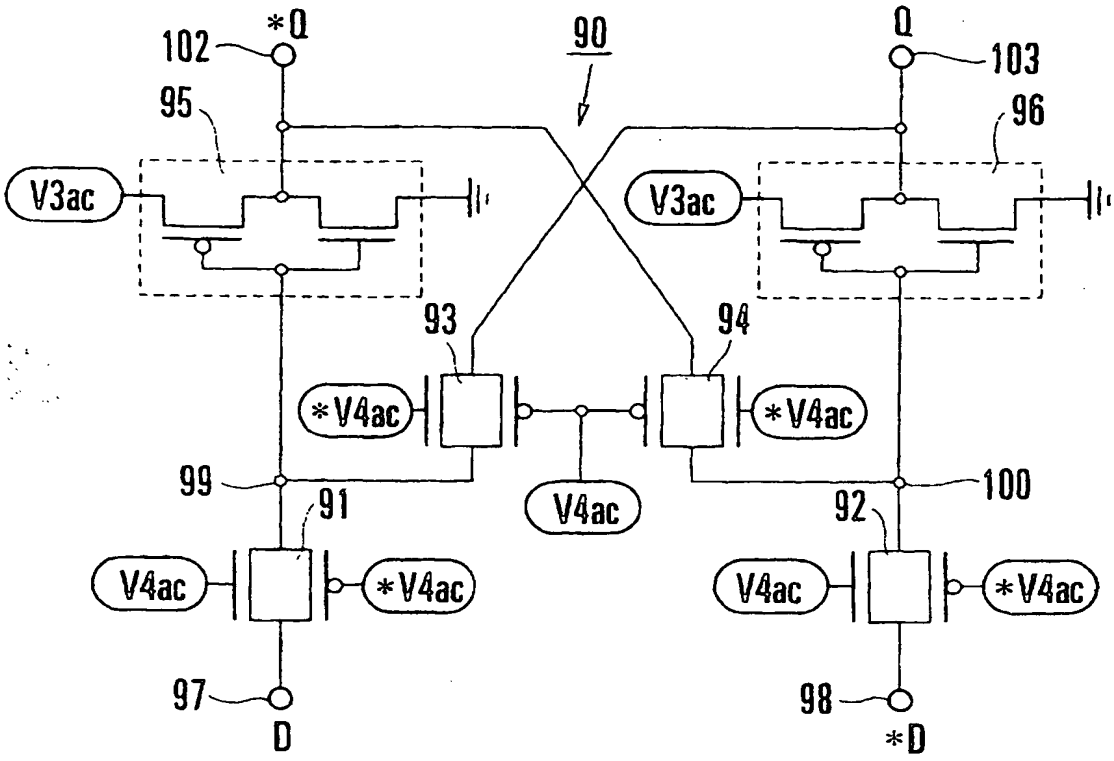
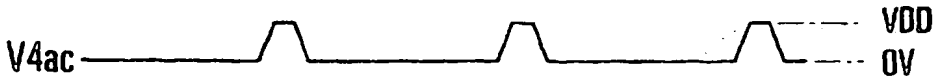


FIG. 44A

FIG. 44B

FIG. 44C



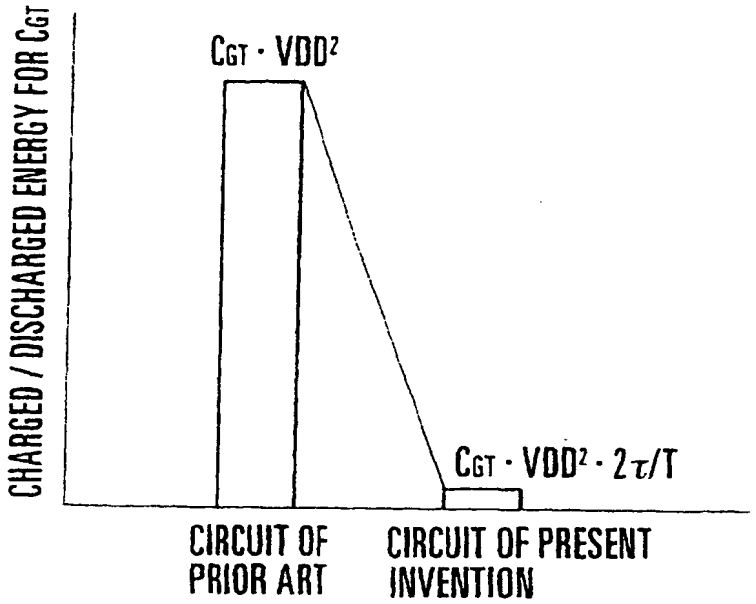


FIG. 45A

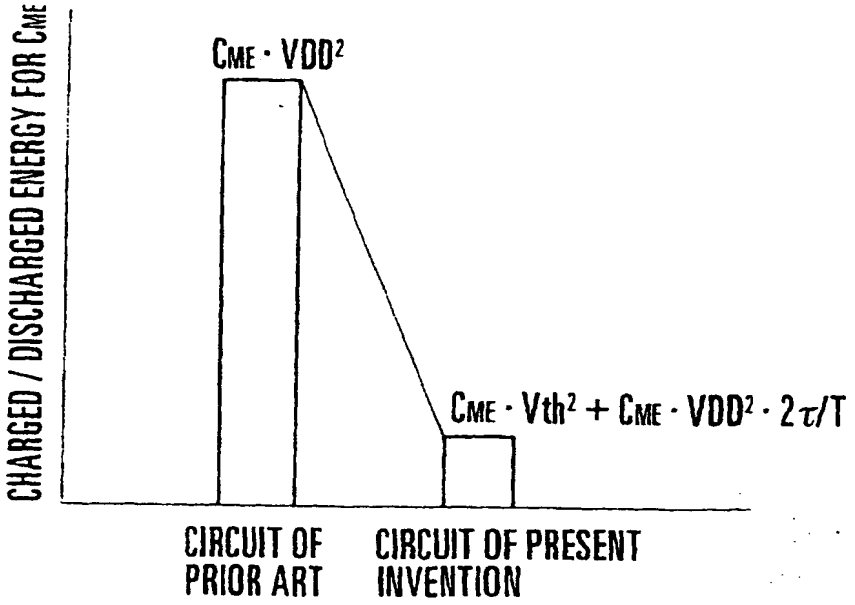


FIG. 45B

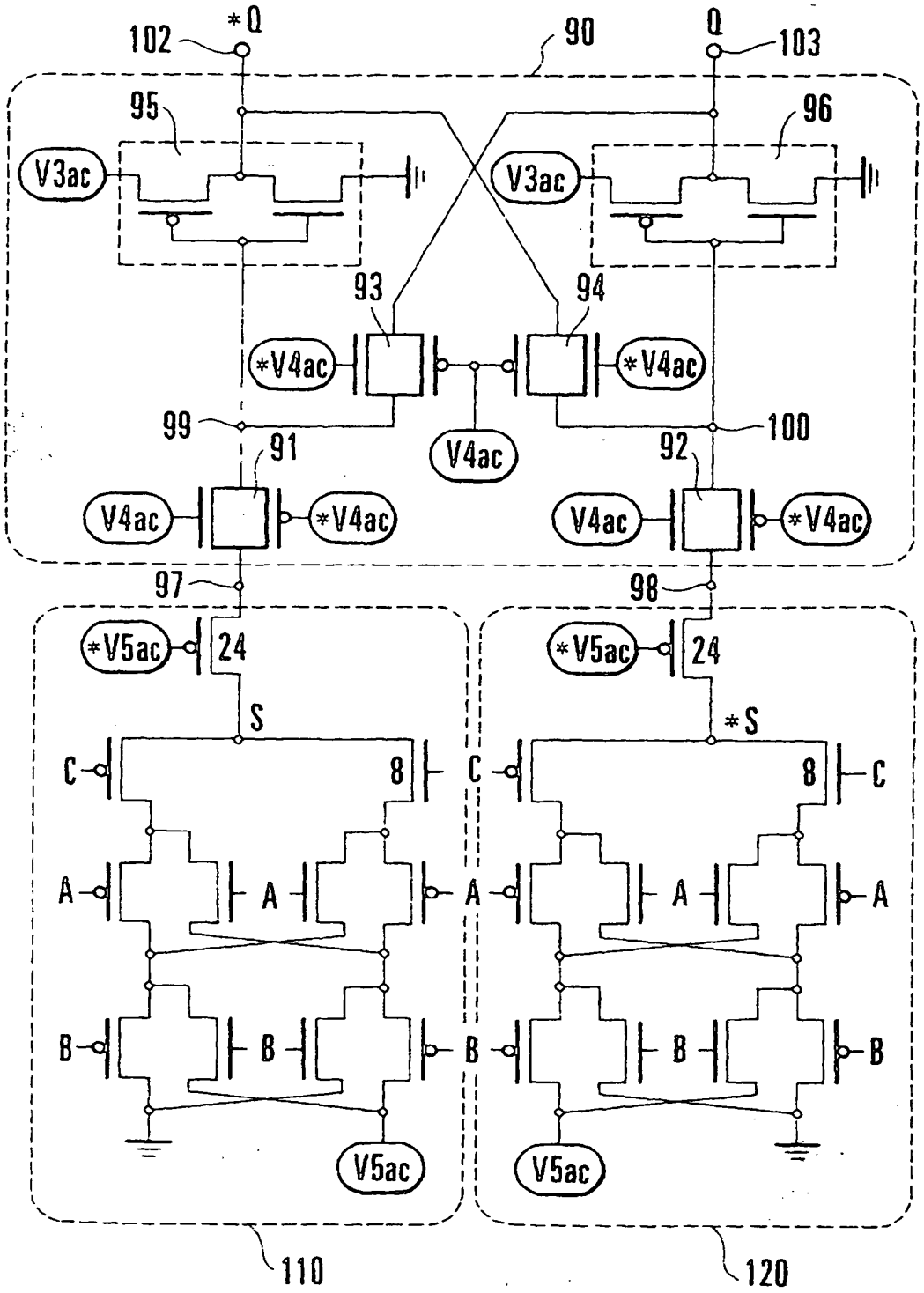


FIG.46

FIG. 47A

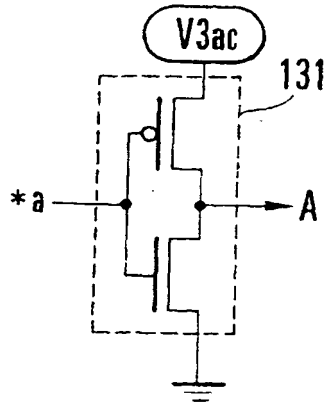


FIG. 47B

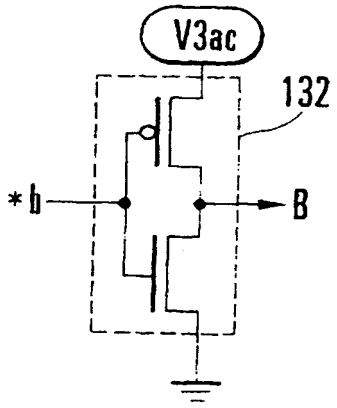


FIG. 47C

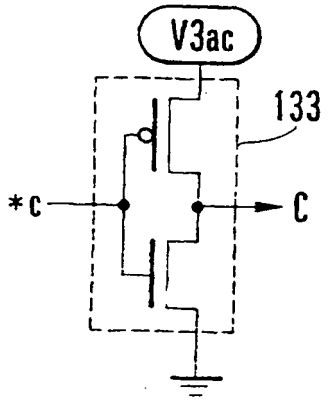


FIG.48A

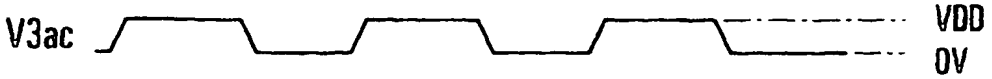


FIG.48B

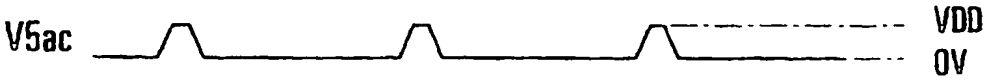


FIG.48C

FIG.48D

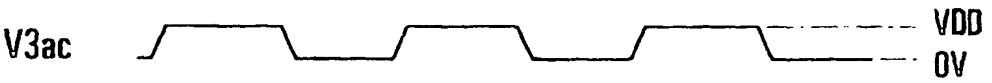


FIG.48E

FIG.48F

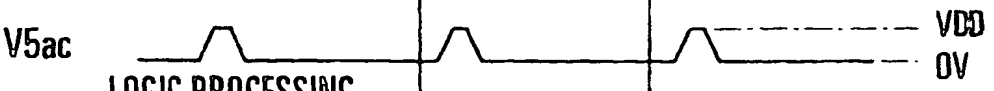
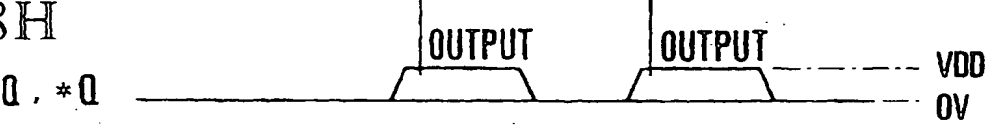


FIG.48G

FIG.48H



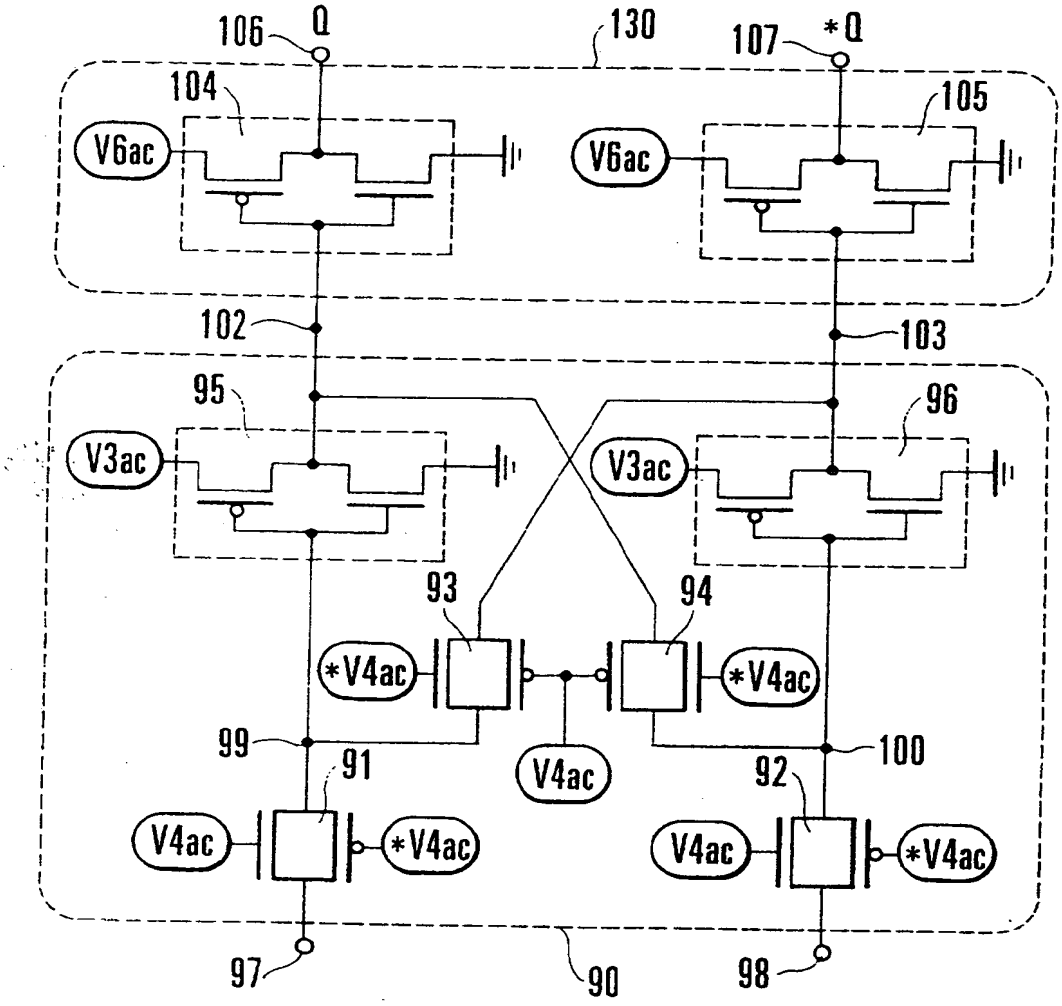
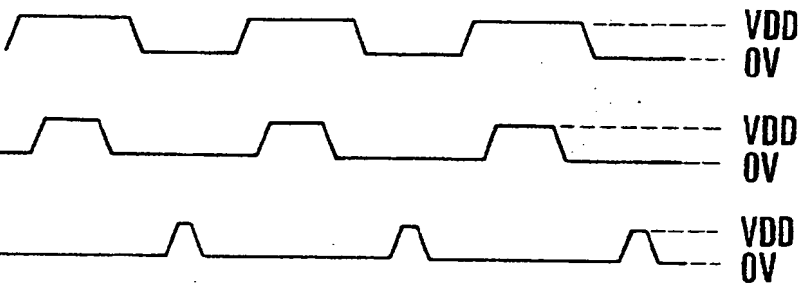


FIG. 49A

FIG. 49B V3ac

FIG. 49C V6ac

FIG. 49D V4ac



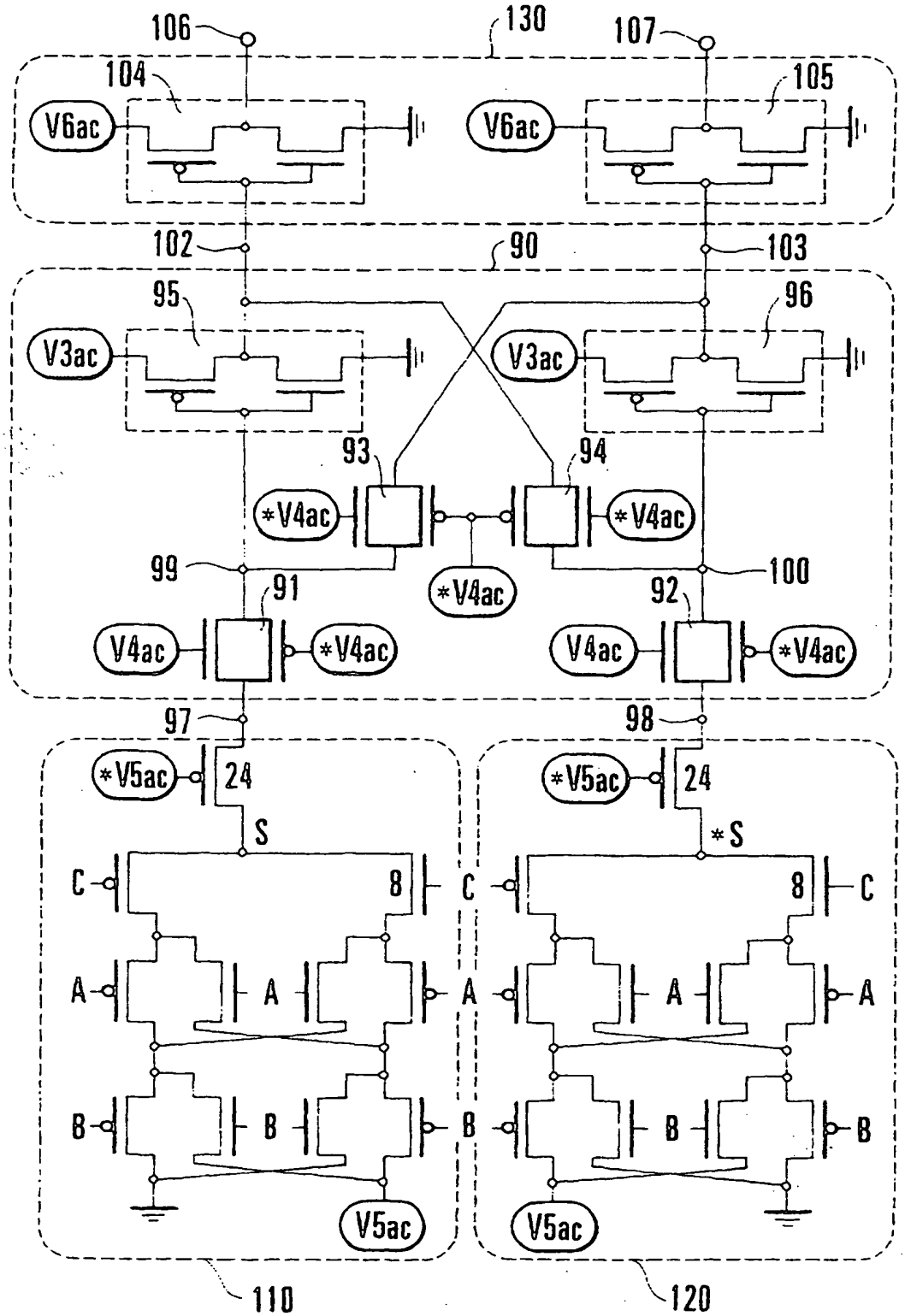


FIG. 50

FIG. 51A

FIG. 51B

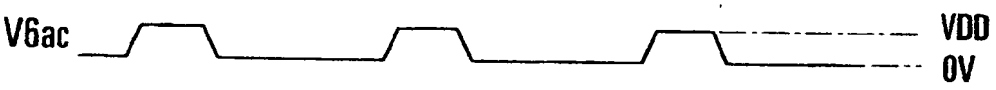


FIG. 51C

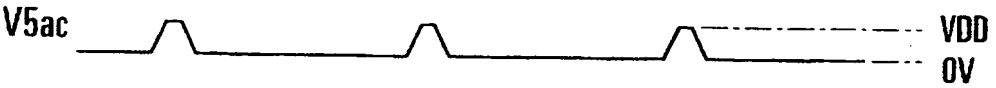
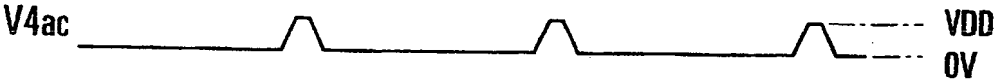


FIG. 51D



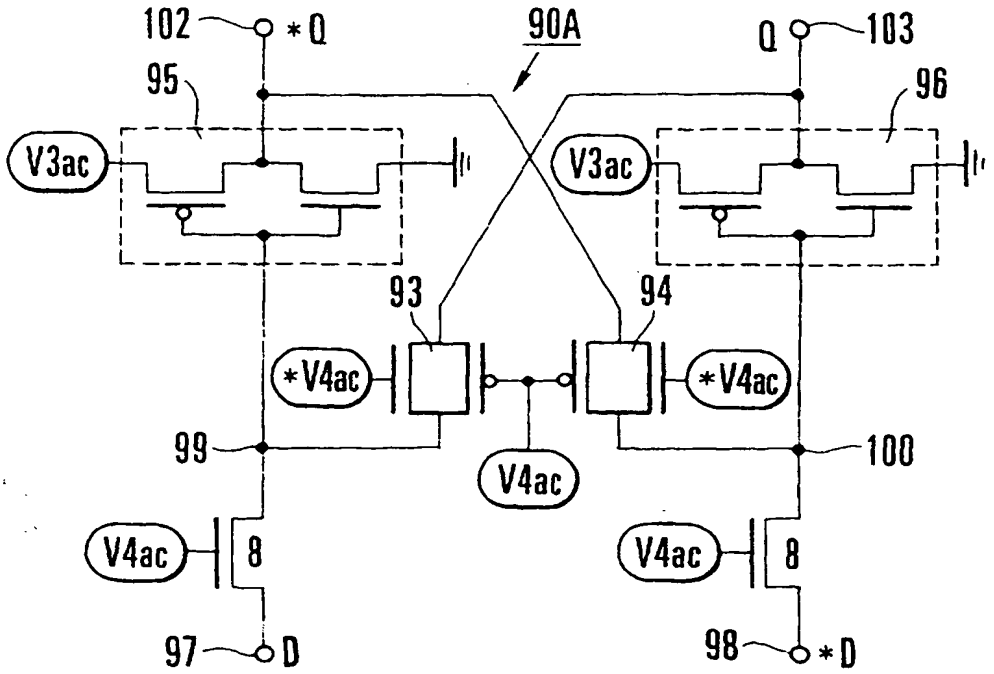


FIG. 52A

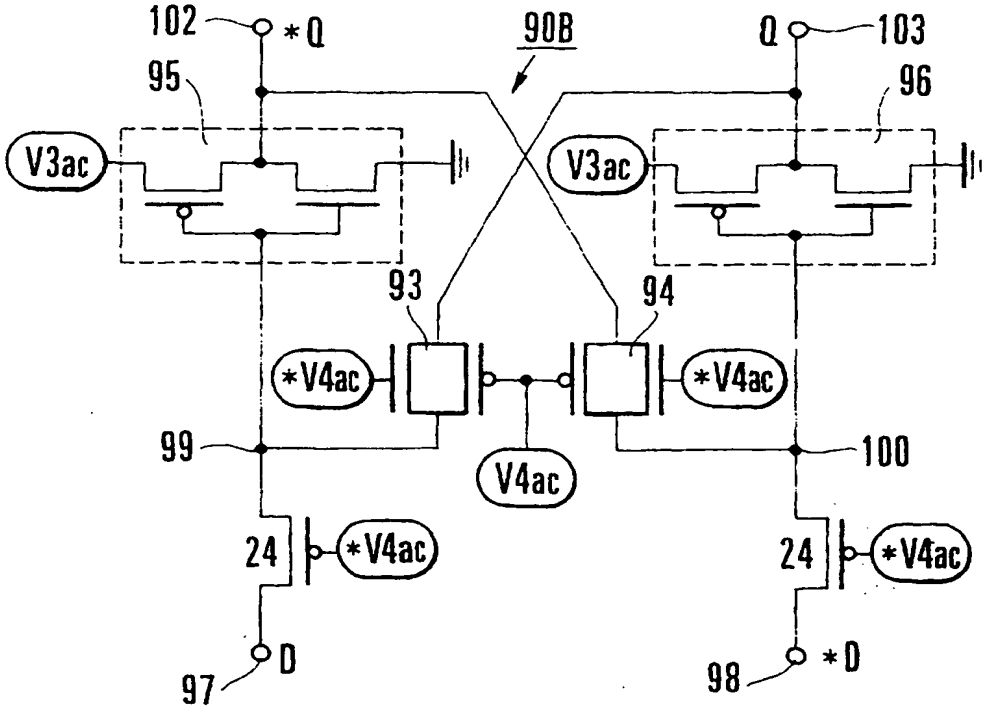


FIG. 52B

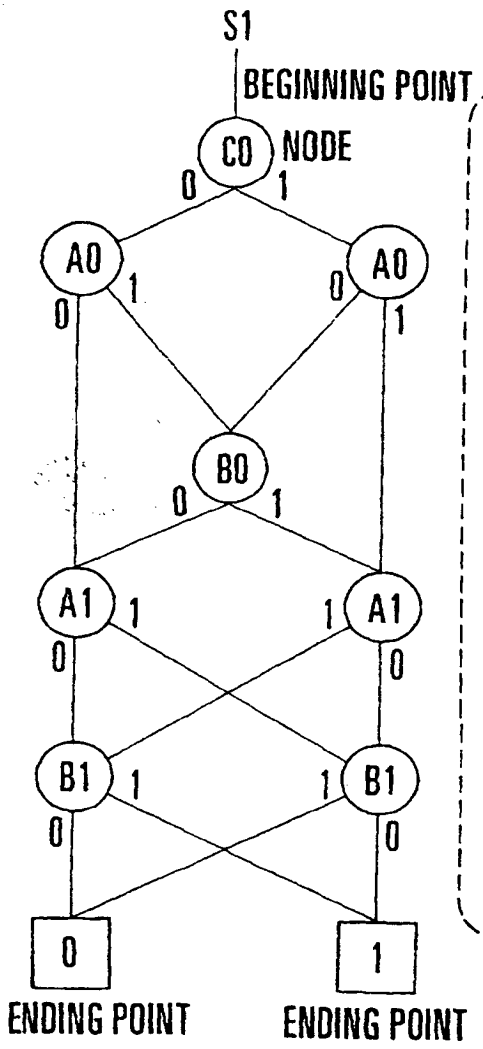


FIG. 53A

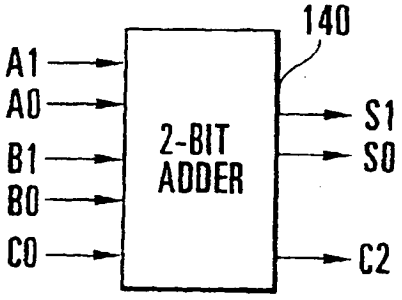


FIG. 53C

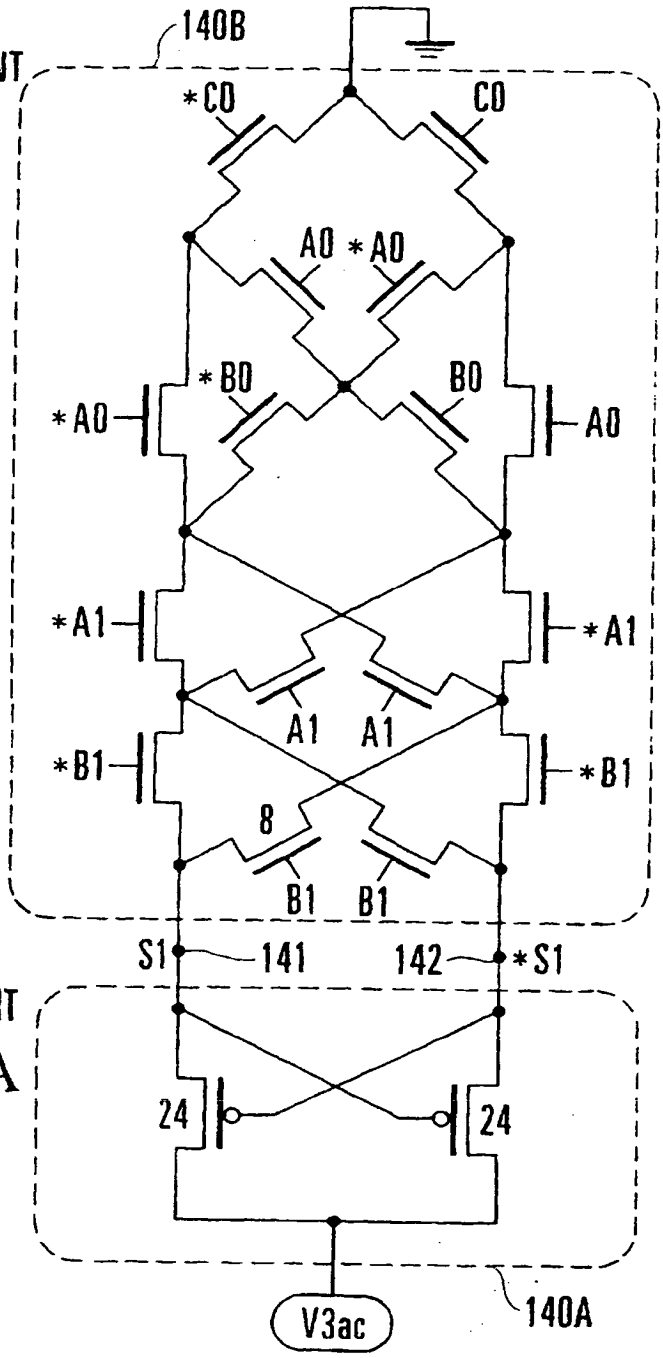


FIG. 53B

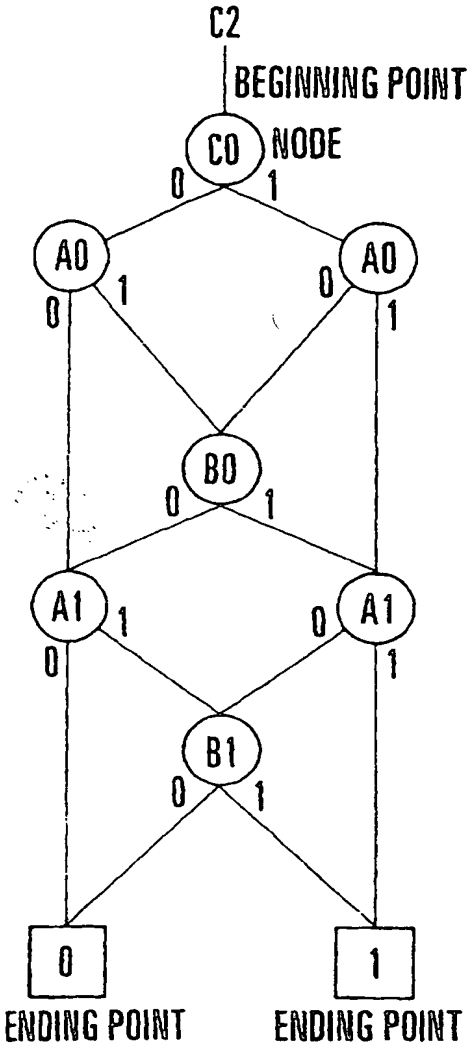


FIG. 54A

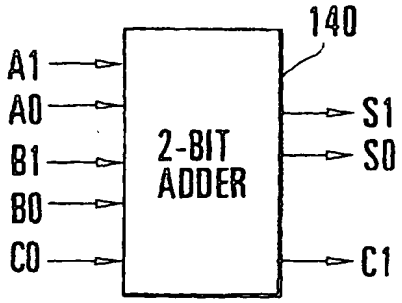


FIG. 54C

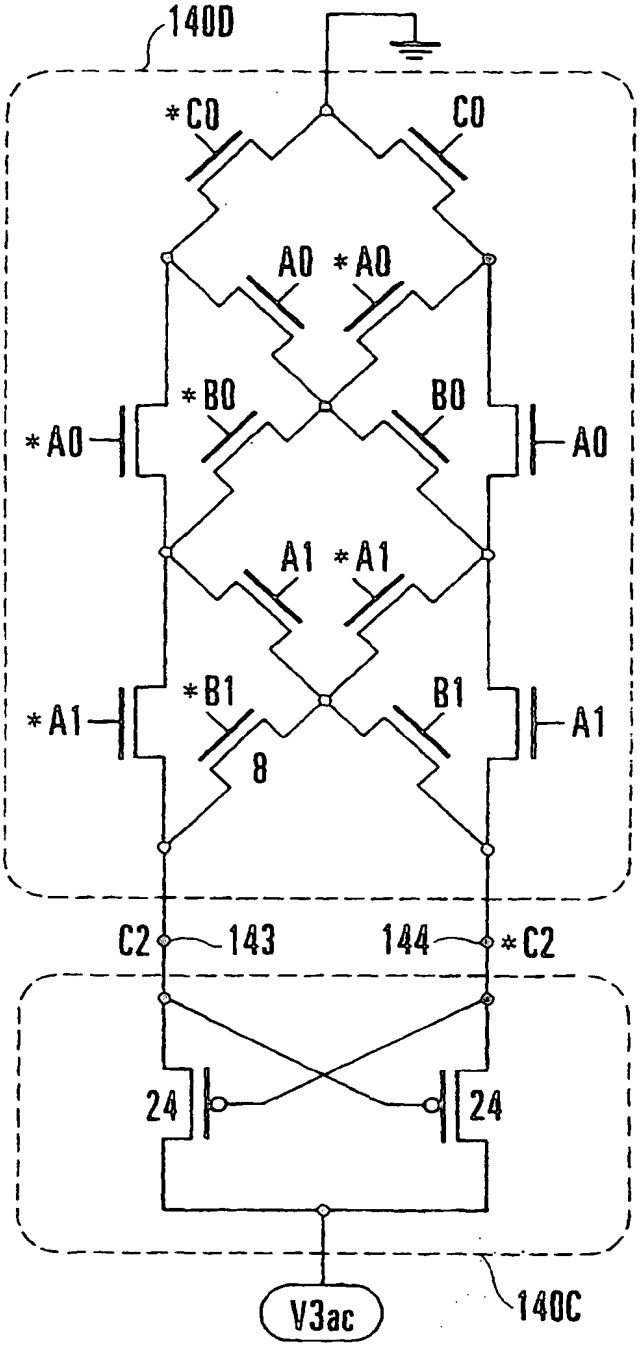


FIG. 54B

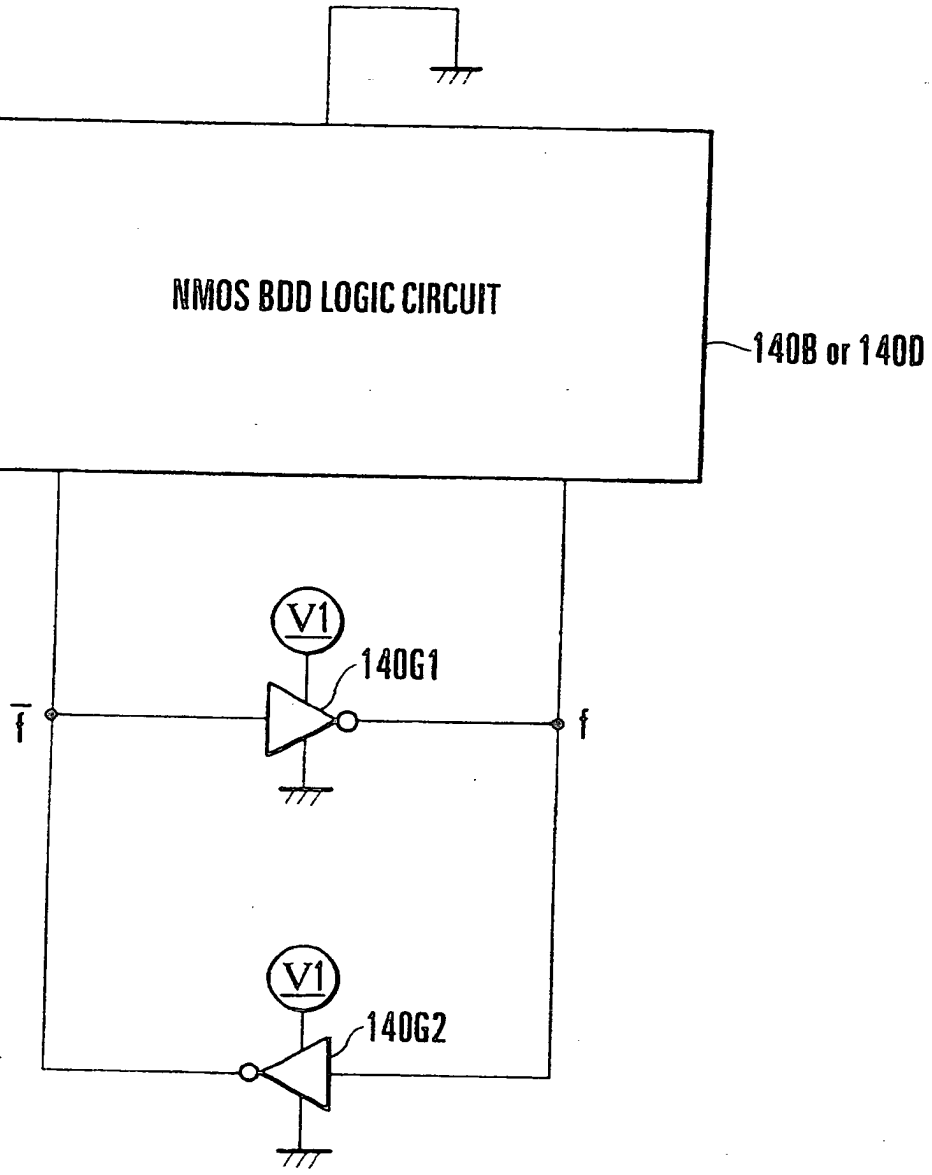


FIG. 55

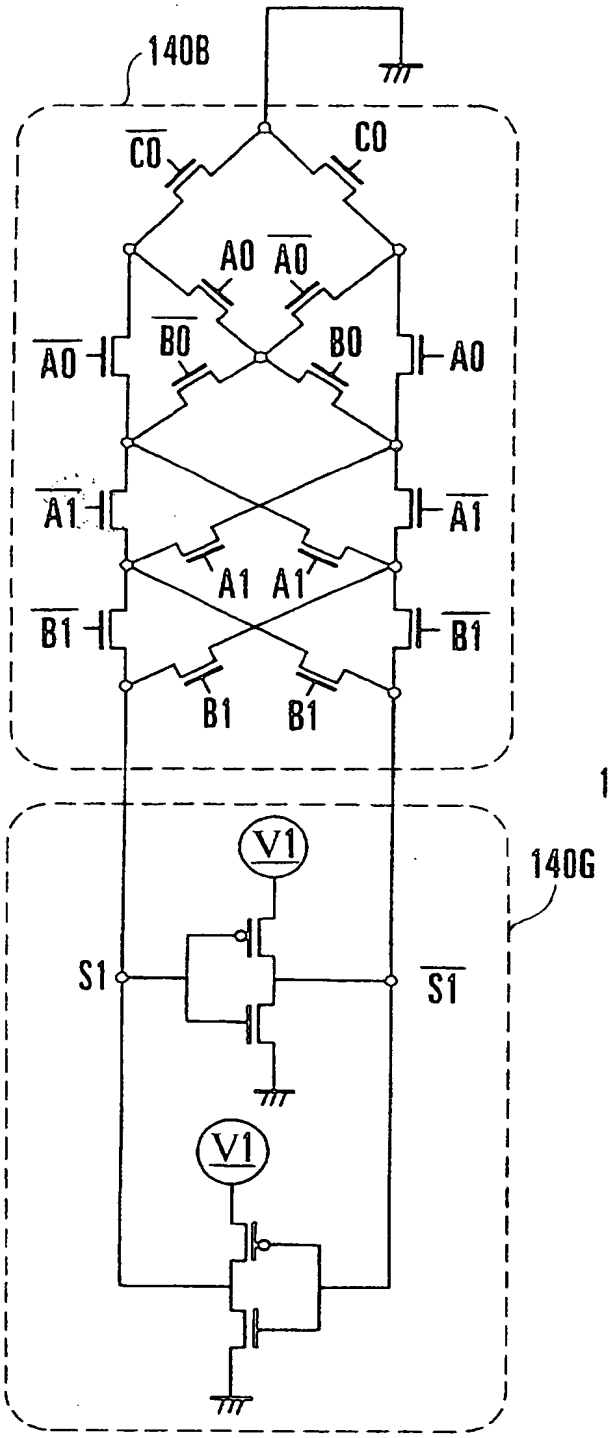


FIG. 56A

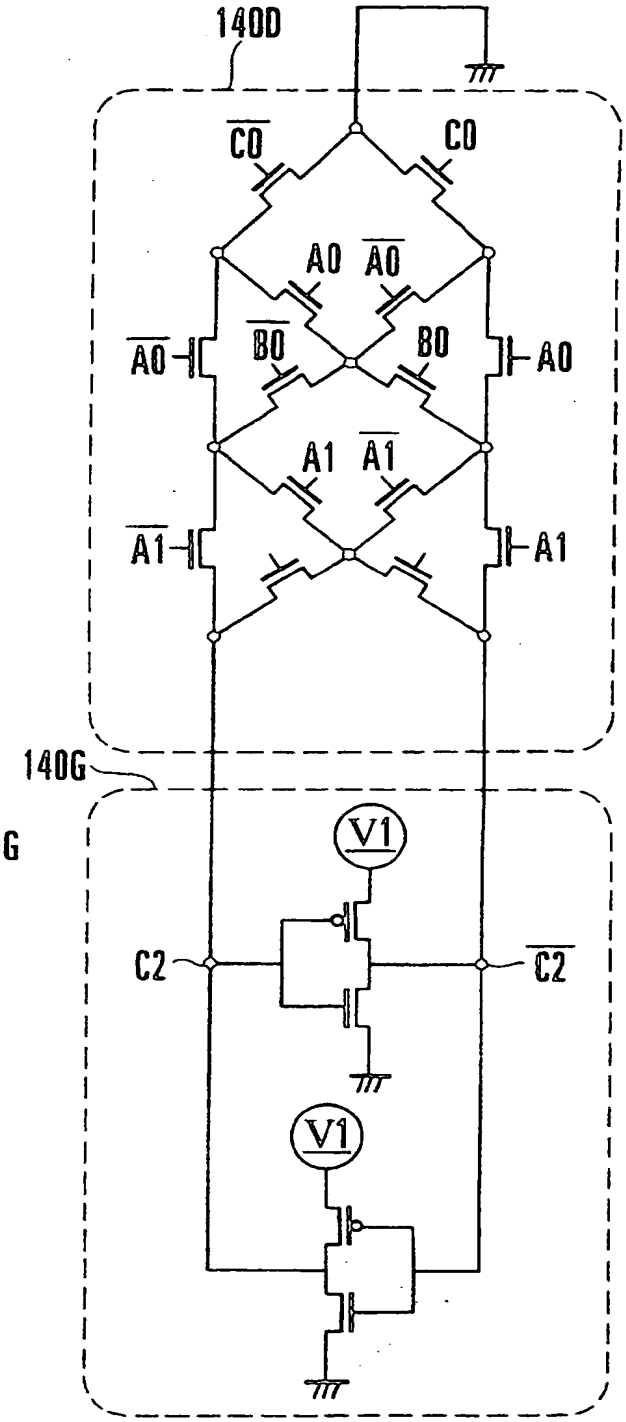


FIG. 56B

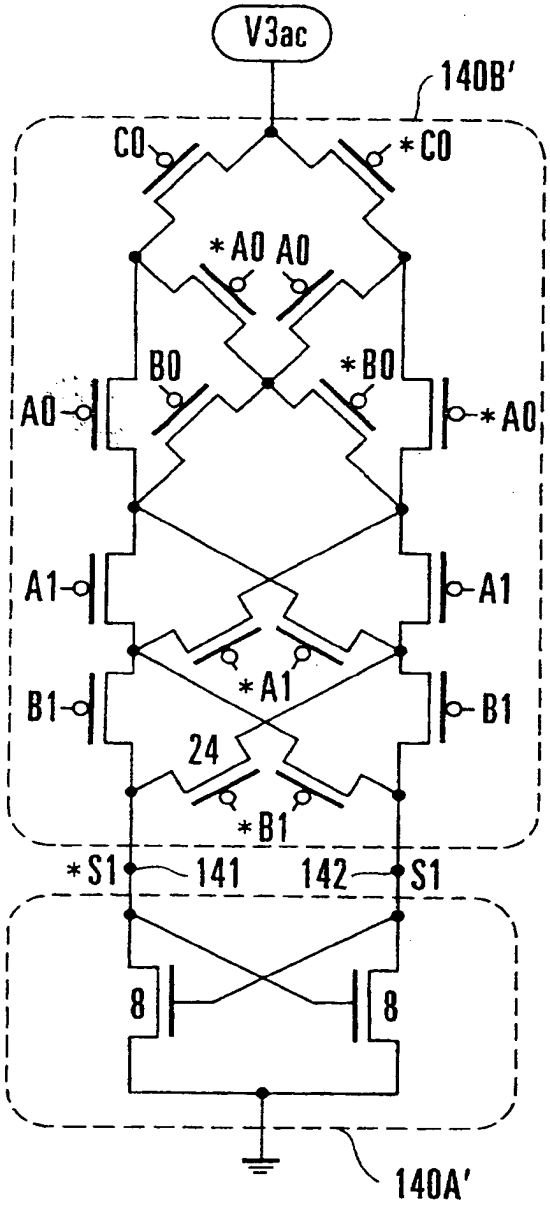


FIG. 57A

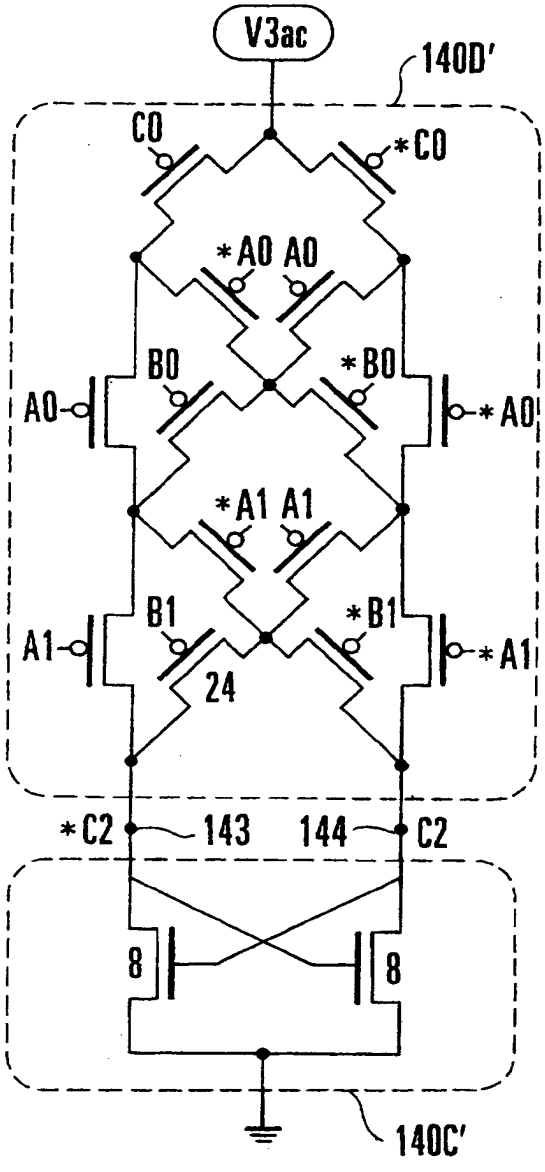


FIG. 57B

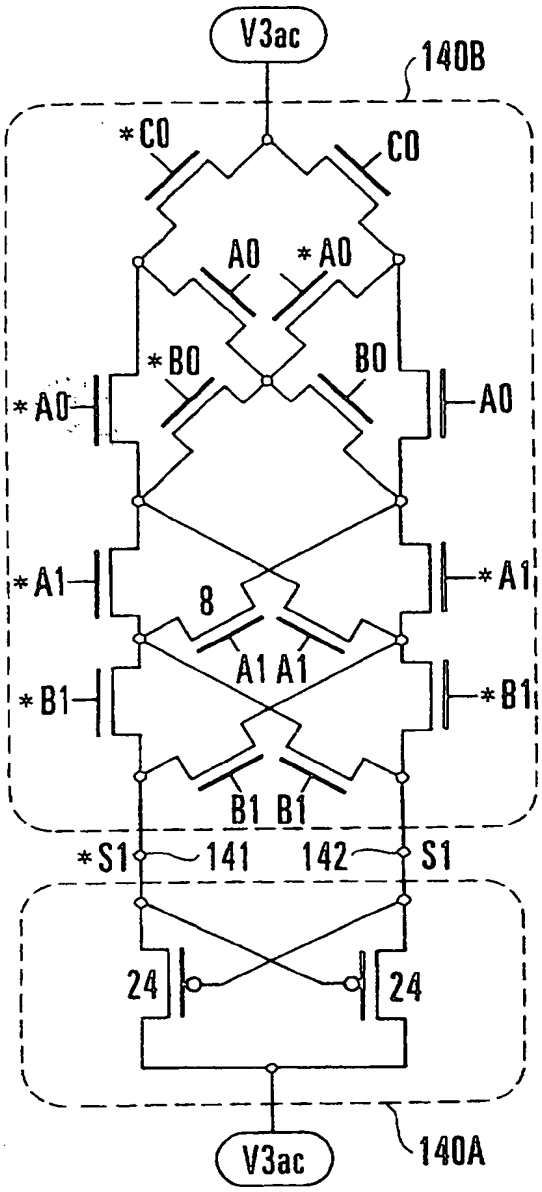


FIG. 58A

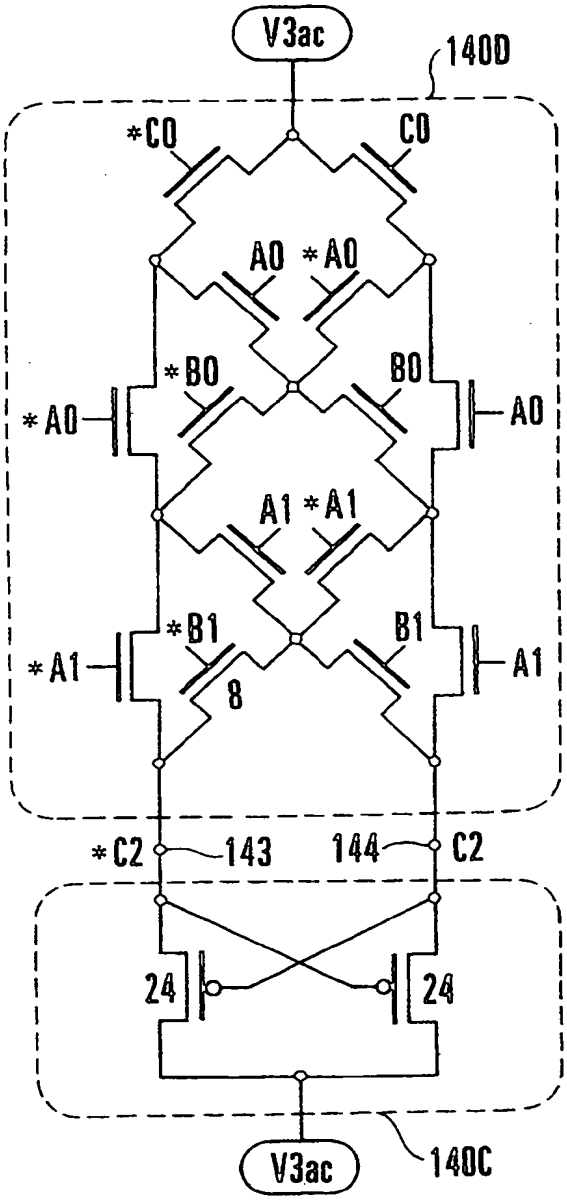


FIG. 58B

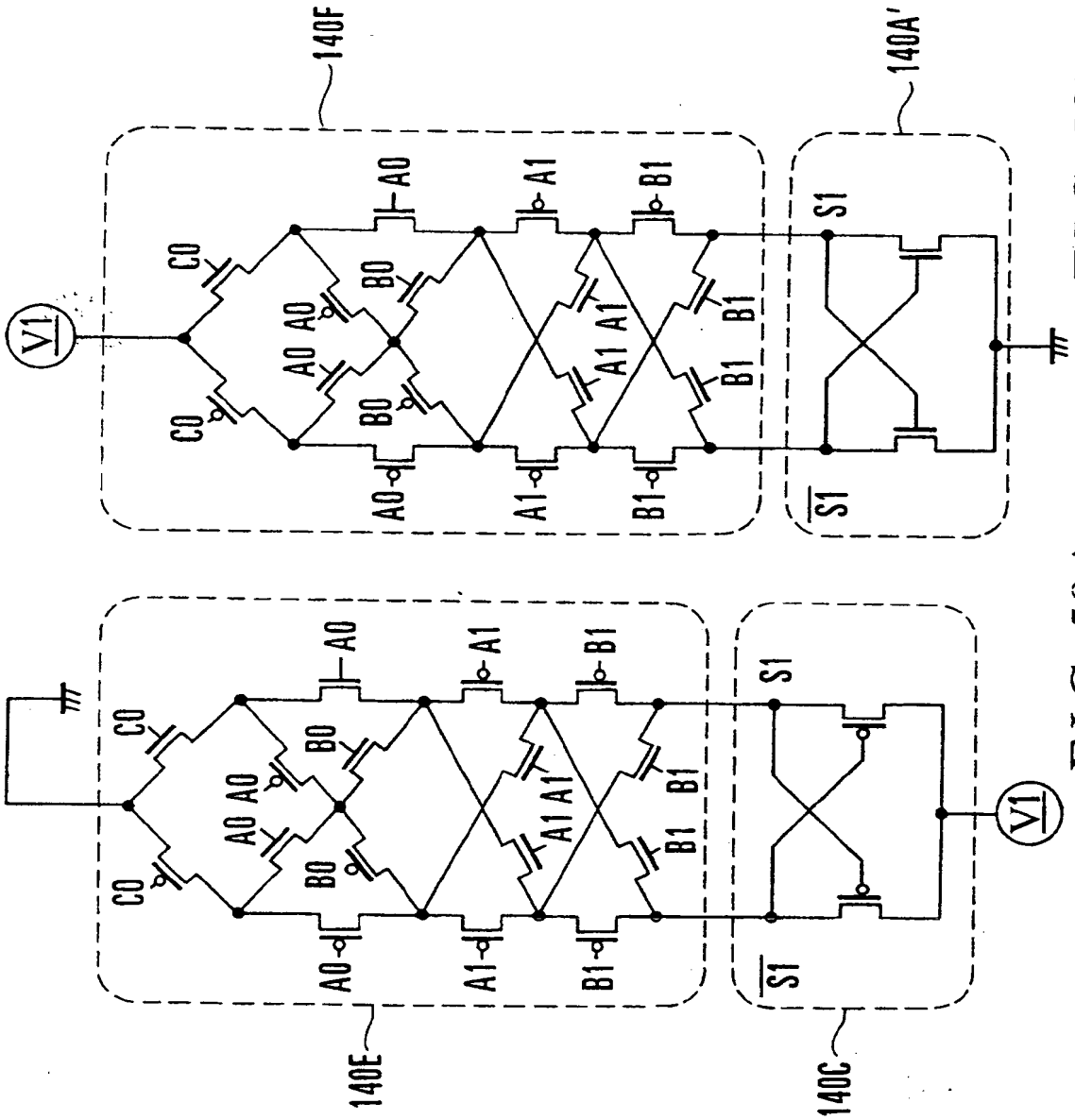


FIG. 59A

FIG. 59B

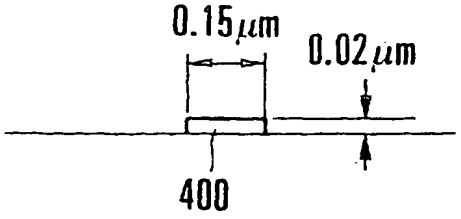


FIG. 60A

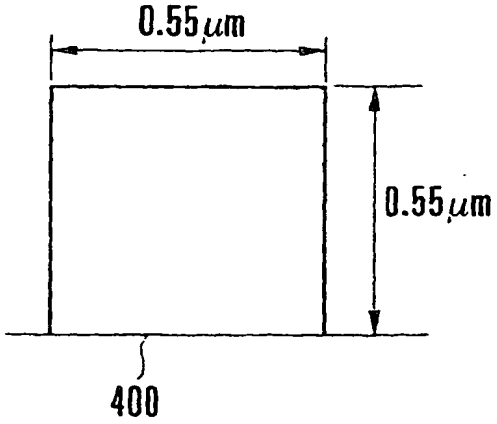


FIG. 60B

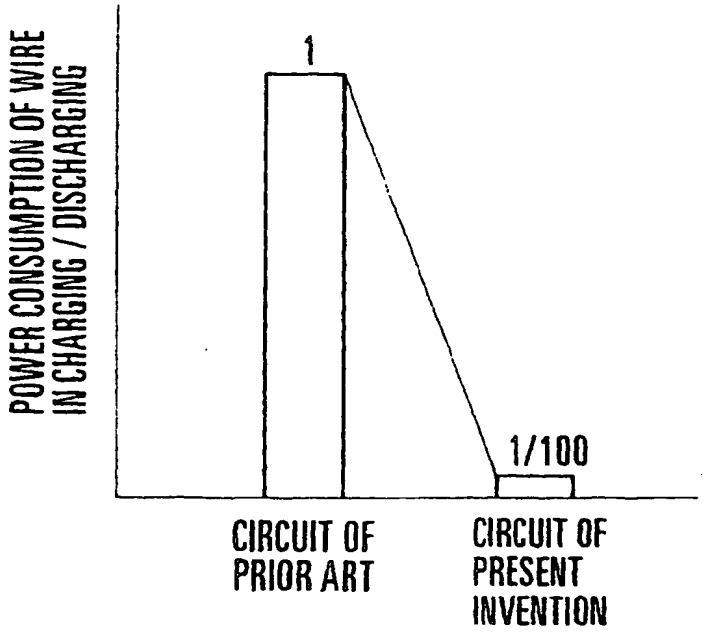


FIG. 60C

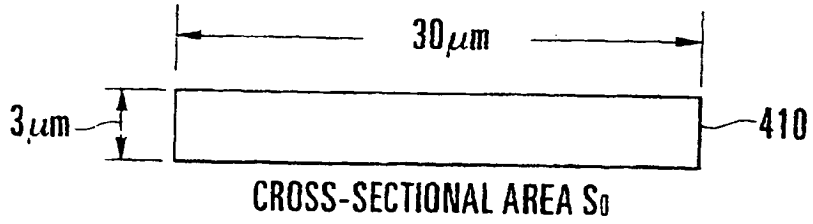


FIG. 61A

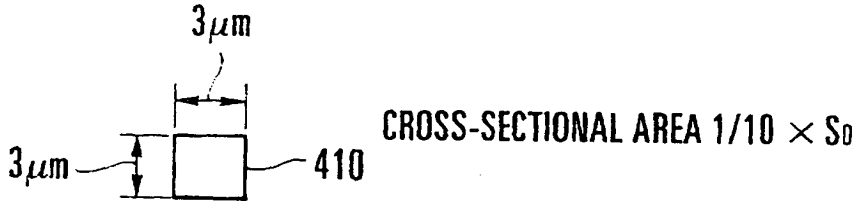


FIG. 61B

FIG. 61C

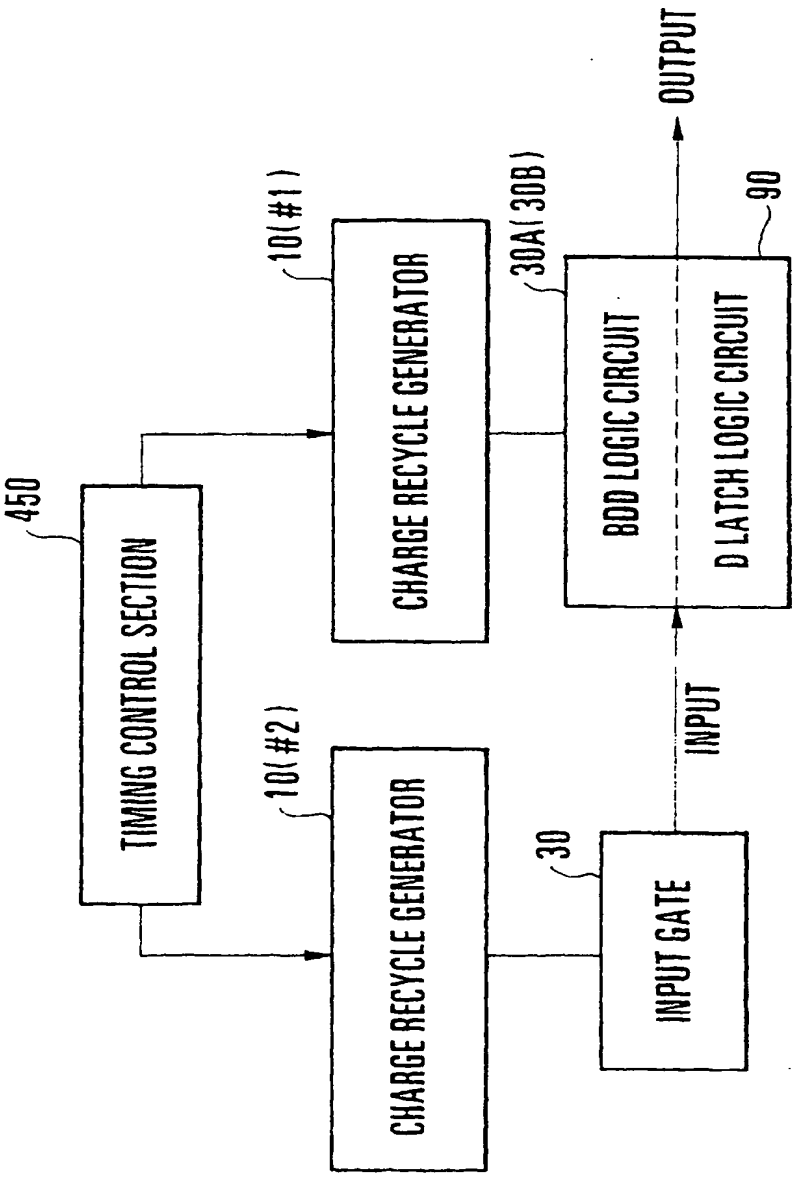


FIG. 62

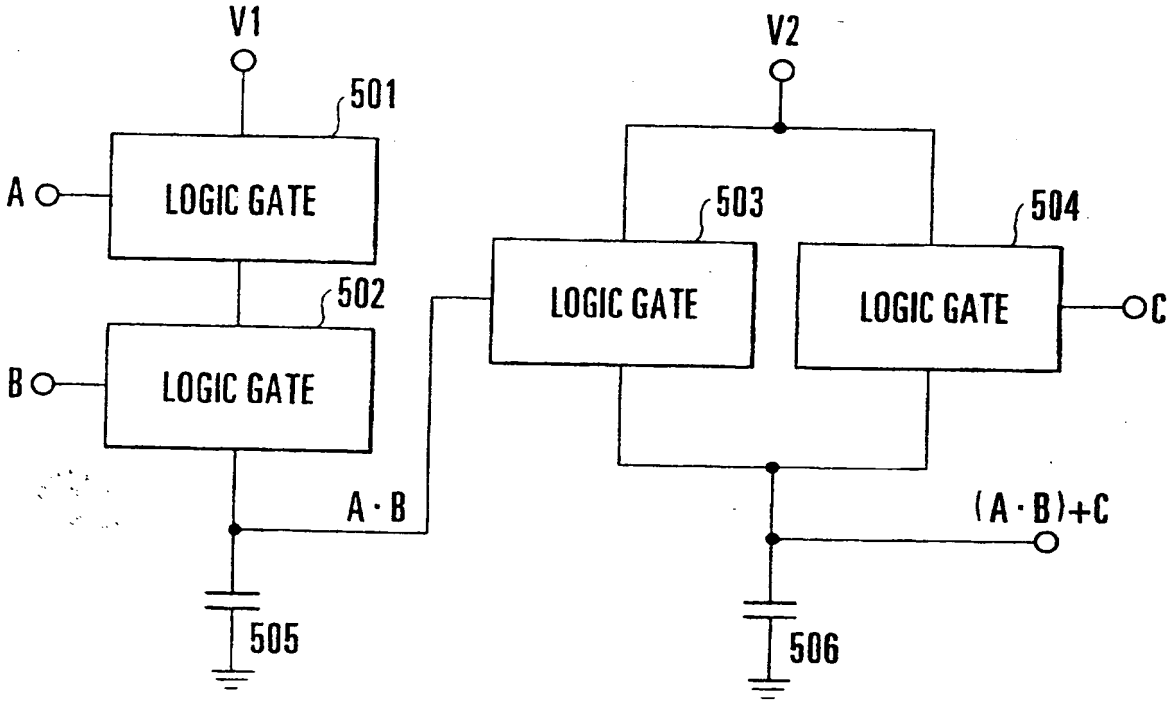


FIG.63A

FIG.63B

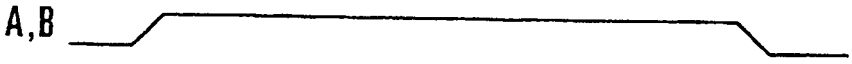


FIG.63C

FIG.63D

FIG.63E

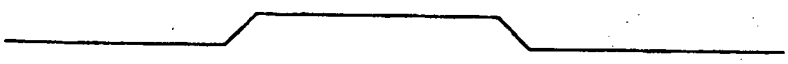
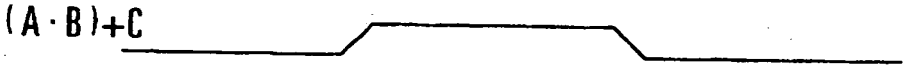


FIG.63F



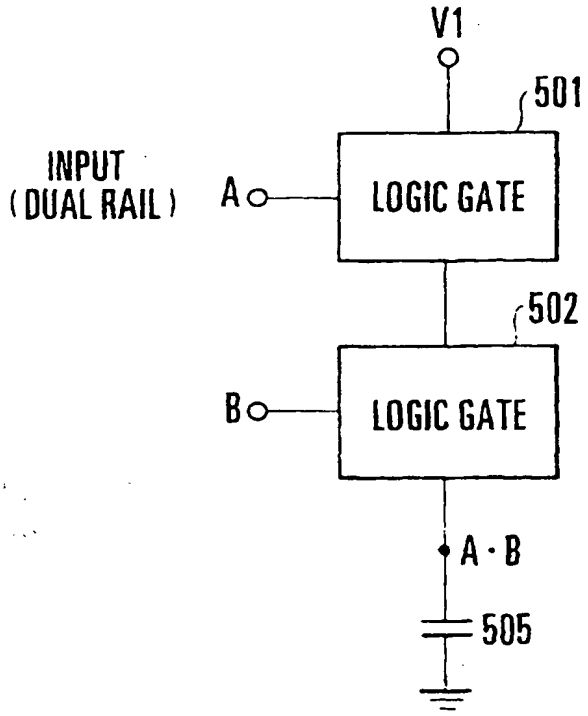


FIG. 64A

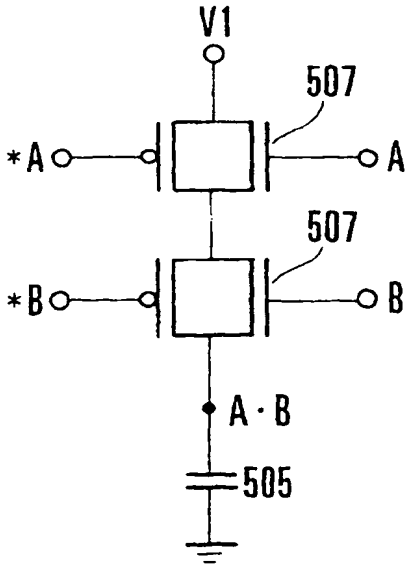


FIG. 64B

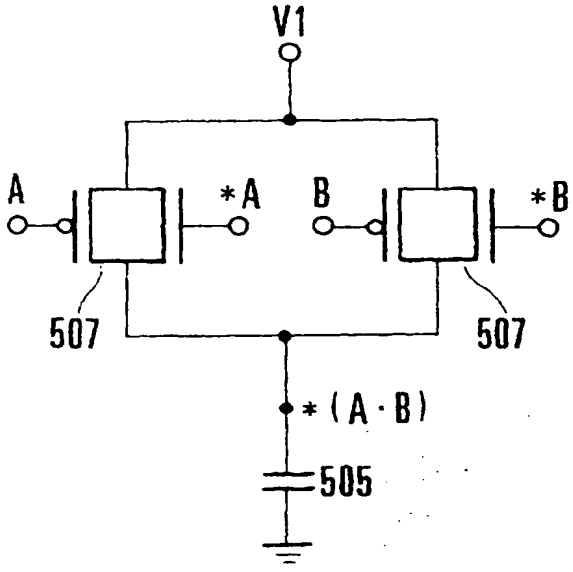


FIG. 64C

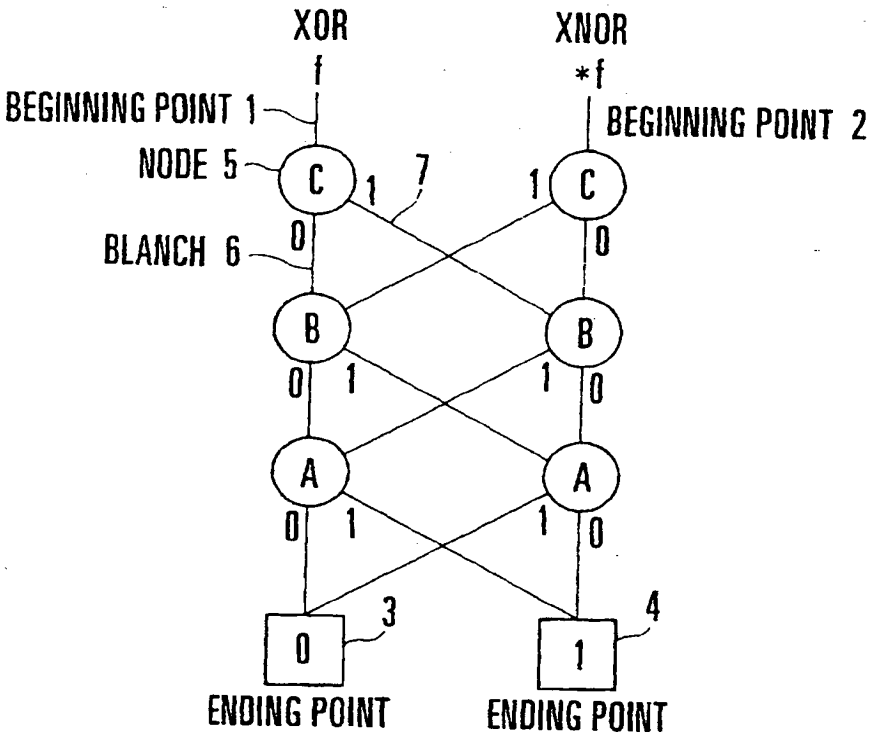


FIG. 65A

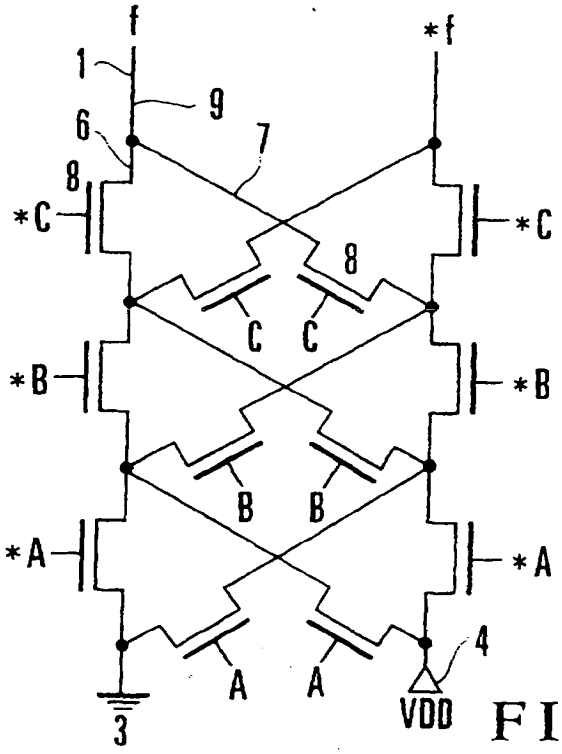


FIG. 65B

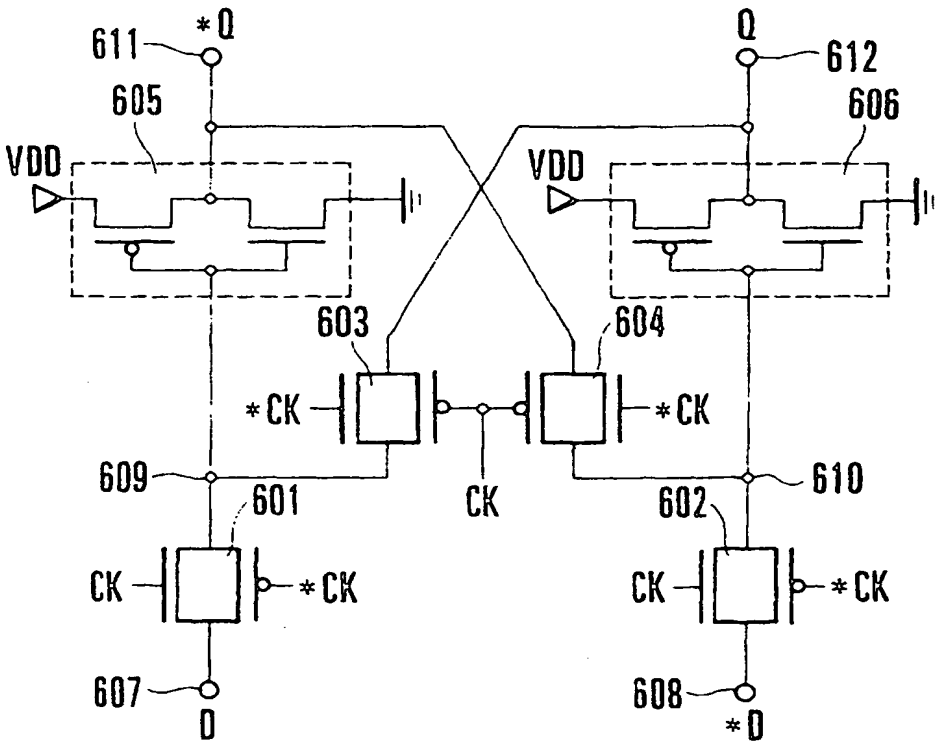


FIG. 66

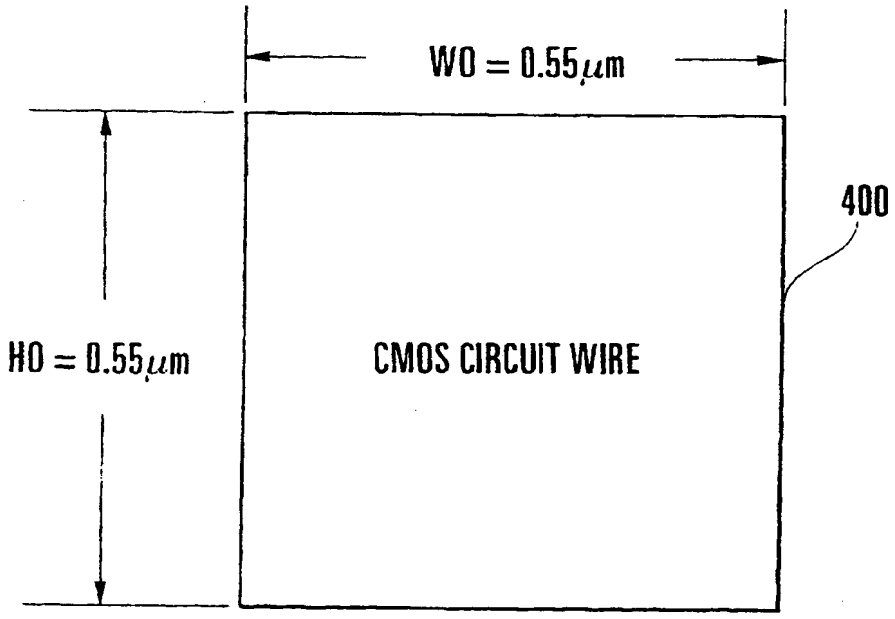


FIG. 67

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EUROPEAN SEARCH REPORT

Application Number
EP 98 25 0308

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	US 5 493 240 A (FRANK DAVID J) 20 February 1996 * column 3, line 58 - column 5, line 52; figures 1,2,9A,9B *	1-3,7,8, 18	H03K19/00
Y		9	
X	US 5 521 538 A (DICKINSON ALEXANDER G) 28 May 1996 * column 2, line 55 - column 4, line 76; figures 1,2 *	1	
Y	* column 6, line 10-53; figures 6,7 *	9	
X	DRAGAN MAKSIMOVIC ET AL: "INTEGRATED POWER CLOCK GENERATORS FOR LOW ENERGY LOGIC" RECORD OF THE ANNUAL POWER ELECTRONICS SPECIALISTS CONFERENCE (PESC, ATLANTA, JUNE 12 - 15, 1995, vol. 1, no. CONF. 26, 12 June 1995, pages 61-67, XP000548387 INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS * figures 1,2,5 *	1,18	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H03K
X	EP 0 685 942 A (AT & T CORP) 6 December 1995 * figures 1,4 *	1	
X	KRAMER A ET AL: "ADIABATIC COMPUTING WITH THE 2N-2N2D LOGIC FAMILY" SYMPOSIUM ON VLSI CIRCUITS. DIGEST OF TECHNICAL PAPERS, HONOLULU, JUNE 9 - 11, 1994,9 June 1994, page 25/26 XP000501008 INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS * the whole document *	1	

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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	16 November 1998	Moll, P

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EUROPEAN SEARCH REPORT

Application Number
EP 98 25 0308

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	HONG Y ET AL: "SAFE BDD MINIMIZATION USING DON'T CARES" PROCEEDINGS OF THE DESIGN AUTOMATION CONFERENCE, ANAHEIM, JUNE 9 - 13, 1997, no. CONF. 34, 9 June 1997, pages 208-213, XP000731844 ASSOCIATION FOR COMPUTING MACHINERY * the whole document *	2-9, 13-17	
A	THORNTON M A ET AL: "BDD-BASED SPECTRAL APPROACH FOR REED-MULLER CIRCUIT REALISATION" IEE PROCEEDINGS: COMPUTERS AND DIGITAL TECHNIQUES, vol. 143, no. 2, 1 March 1996, pages 145-150, XP000594714 * the whole document *	2-9, 13-17	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	16 November 1998	Moll, P

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16-11-1998

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5493240 A	20-02-1996	NONE	
US 5521538 A	28-05-1996	CA 2172096 A	01-10-1996
		EP 0735688 A	02-10-1996
		JP 8335873 A	17-12-1996
EP 0685942 A	06-12-1995	US 5506519 A	09-04-1996
		JP 7336206 A	22-12-1995

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